

Description

The CY6N137 optocoupler consists of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photodetector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10kV/μs. The CY6N137 has a minimum CMR of 5kV/μs.

Features

- Very high speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Storable output
- Wired OR-open collector

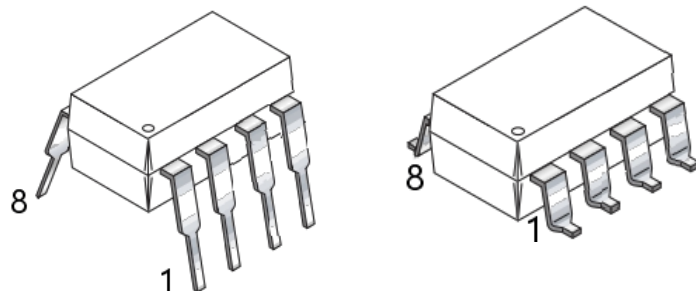
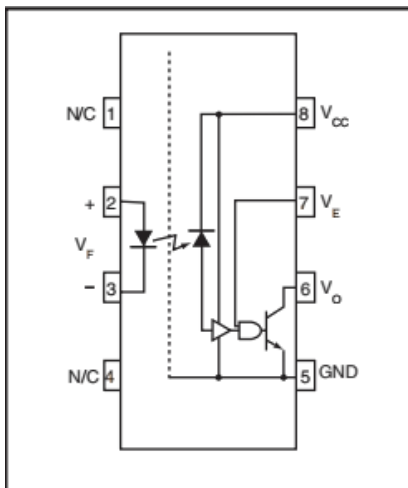
Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Block Diagram and Package



Absolute Maximum Ratings (Ta=25°C)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Unit
TSTG	Storage Temperature	-55 to +125	°C
TOPR	Operating Temperature	-40 to +85	°C
TSOL	Lead Solder Temperature (for wave soldering only)	260 for 10 sec	°C
EMITTER			
IF	DC/Average Forward Input Current	50	mA
VE	Enable Input Voltage Not to Exceed VCC by more than 500mV	5.5	V
VR	Reverse Input Voltage	5.0	V
PI	Power Dissipation	100	mW
DETECTOR			
VCC (1 minute max)	Supply Voltage	7.0	V
IO	Output Current	50	mA
VO	Output Voltage	7.0	V
PO	Collector Output	85	mW

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We do not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	IFL	0	250	A
Input Current, High Level	IFH	*6.3	15	mA
Supply Voltage, Output	VCC	4.5	5.5	V
Enable Voltage, Low Level	VEL	0	0.8	V
Enable Voltage, High Level	VEH	2.0	VCC	V
Operating Temperature	TA	-40	85	°C
Fan Out (TTL Load)	N		8	

Note: *6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electro-optical Characteristics (Ta=0 to 70°C unless otherwise specified)
Individual Component Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
EMITTER						
Input Forward Voltage	VF	IF = 10mA TA = 25°C		1.4	1.8 1.75	V
Input Reverse Breakdown Voltage	BVR	IR = 10μA	5.0			V
Input Capacitance	CIN	VF = 0, f = 1MHz		60		pF
Input Diode Temperature Coefficient	ΔVF/ΔTA	IF = 10mA		-1.4		mV/°C
DETECTOR						
High Level Supply Current	ICCH	VCC = 5.5V, IF = 0mA, VE = 0.5V		7	10	mA
Low Level Supply Current	ICCL	VCC = 5.5V, IF = 10mA		9	13	mA
Low Level Enable Current	IEL	VCC = 5.5V, VE = 0.5V		-0.8	-1.6	mA
High Level Enable Current	IEH	VCC = 5.5V, VE = 2.0V		-0.6	-1.6	mA
High Level Enable Voltage	VEH	VCC = 5.5V, IF = 10mA	2.0			V
Low Level Enable Voltage	VEL	VCC = 5.5V, IF = 10mA (3)			0.8	V

Switching Characteristics (TA -40°C to +85°C, VCC= 5V, IF= 7.5mA unless otherwise specified)

AC Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time to Output HIGH Level	TPLH	CL=15pF (4)(Fig. 11) RL = 350 Ω , TA = 25°C	20	45	100 75	ns
Propagation Delay Time to Output LOW Level	TPHL	TA = 25°C (5) RL = 350 Ω , CL= 15pF (Fig. 11)	25	45	75 100	ns
Pulse Width Distortion	TPHL – TPLH	(RL = 350 Ω , CL=15pF (Fig. 11)		3	35	ns
Output Rise Time (10–90%)	tr	RL = 350 Ω , CL = 15pF(6) (Fig. 11)		50		ns
Output Fall Time (90–10%)	tf	RL = 350 Ω , CL = 15pF(7) (Fig. 11)		12		ns
Enable Propagation Delay Time to Output HIGH Level	tELH	IF = 7.5mA, VEH = 3.5V, RL = 350Ω ,CL = 15pF (8)		20		ns
Enable Propagation Delay Time to Output LOW Level	tEHL	IF = 7.5mA, VEH = 3.5V, RL = 350Ω,CL = 15pF(9)		20		ns
Common Mode Transient Immunity (at Output HIGH Level)	CMH	TA = 25°C, VCM = 50V (Peak), IF = 0mA, VOH (Min.) = 2.0V, RL = 350Ω(10) (Fig. 12)	5000	10000		V/μs
Common Mode Transient Immunity (at Output LOW Level)	CML	RL = 350Ω, IF = 7.5mA, VOL (Max.) = 0.8V, TA = 25°C(11) (Fig. 1 2)	5000	10000		V/μs

Electrical Characteristics (Continued)
Transfer Characteristics (TA = -40 to +85°C unless otherwise specified)

DC Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
HIGH Level Output Current	IOH	VCC = 5.5V, VO = 5.5V, IF = 250μA, VE = 2.0V(2)			100	μA

DC Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
LOW Level Output Current	VOL	VCC = 5.5V, IF = 5mA, VE = 2.0V, ICL = 13mA(2)		0.35	0.6	V
Input Threshold Current	IFT	VCC = 5.5V, VO = 0.6V, VE = 2.0V, IOL = 13mA		3	5	mA

Isolation Characteristics (TA = -40°C to +85°C unless otherwise specified.)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input-Output Insulation Leakage Current	II-O	Relative humidity = 45%, TA = 25°C, t = 5s, VI -O = 3000 VDC(12)			10*	μA
Withstand Insulation Test Voltage	VISO	RH < 50%, TA = 25° C, II-O ≤ 2μA, t = 1 min. (12)	2500			VRMS
Resistance (Input to Output)	RI-O	VI-O = 500V(12)		1012		Ω
Capacitance (Input to Output)	CI-O	f = 1MHz(12)		0.6		pF

* All Typical at VCC = 5V, TA = 25°C

Note:

- The VCC supply to each optoisolator must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins of each device.
- One channel.
- Enable Input – No pull up resistor required as the device has an internal pull up resistor.
- tPLH – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- tPHL – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- tr – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- tf – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- tELH – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- tEHL – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- CMH – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., VOUT > 2.0V).
Measured in volts per microsecond (V/μs).
- CML – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., VOUT < 0.8V). Measured in volts per microsecond (V/μs).
- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

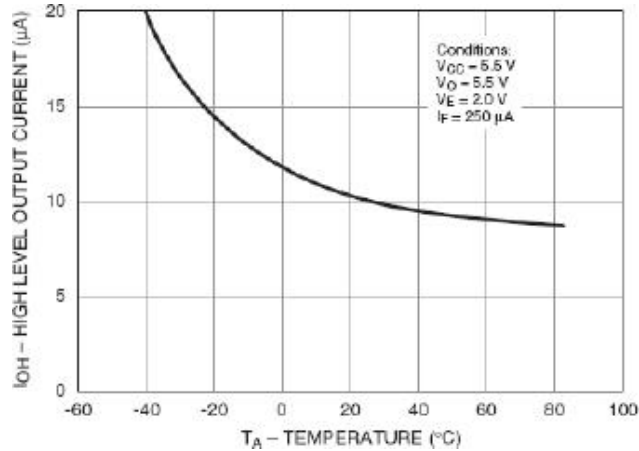


Fig.1 High Level Output Current VS Temperature

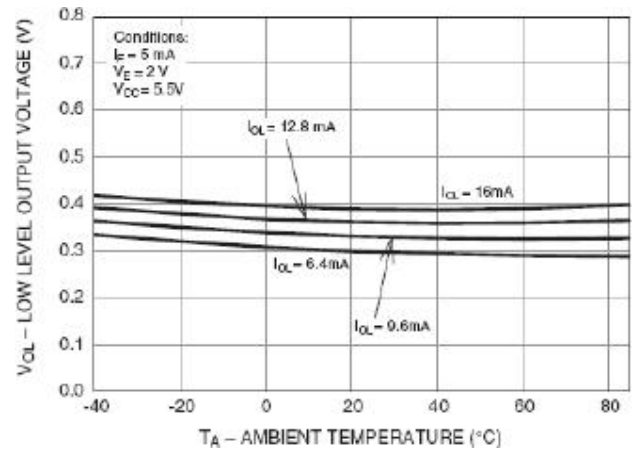


Fig.2 Low Level Output Voltage VS Temperature

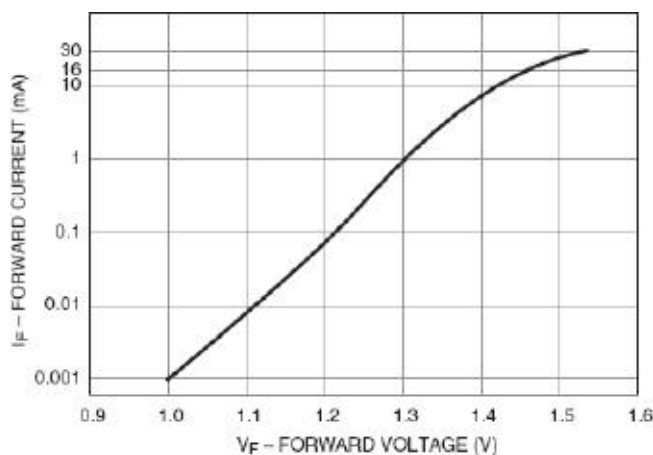


Fig.3 Input Diode Forward Characteristic

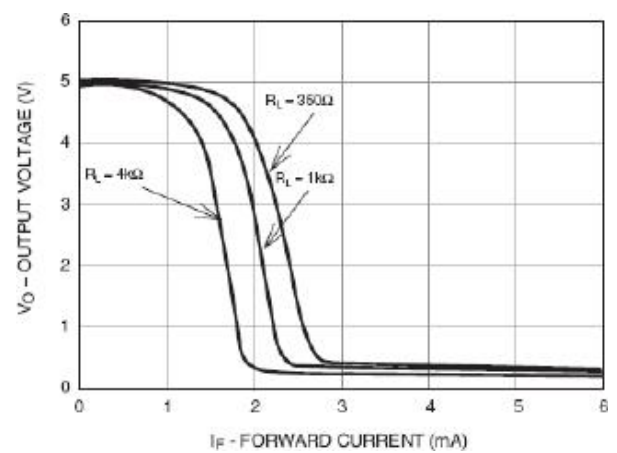


Fig.4 Output Voltage VS Forward Input Current

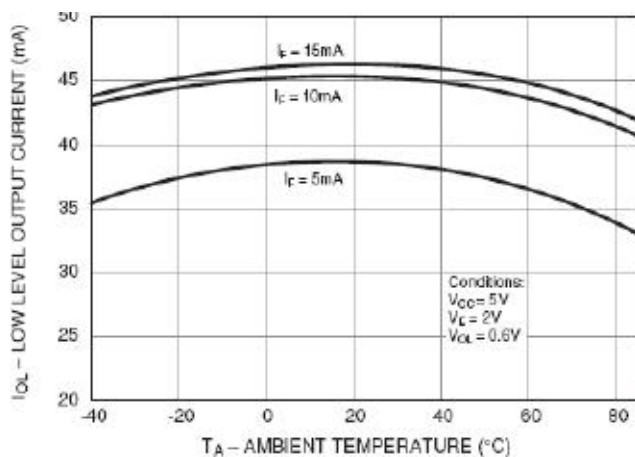


Fig.5 Low Level Output Current VS Temperature

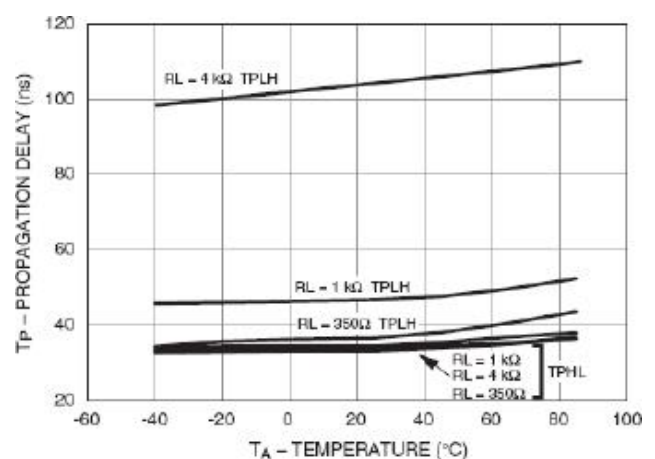


Fig.6 Propagation Delay VS Temperature

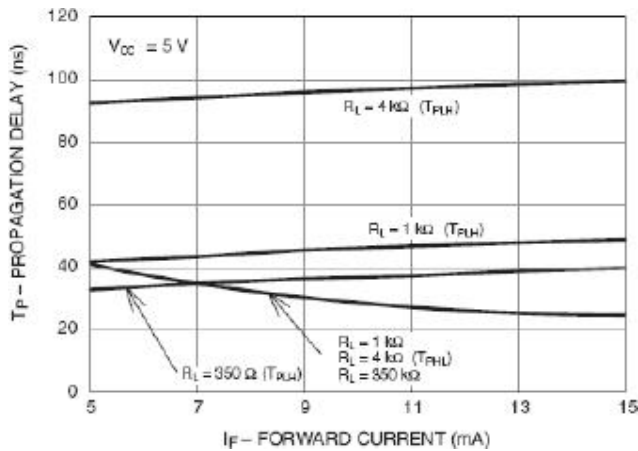


Fig.7 Propagation Delay VS Pulse Input Current

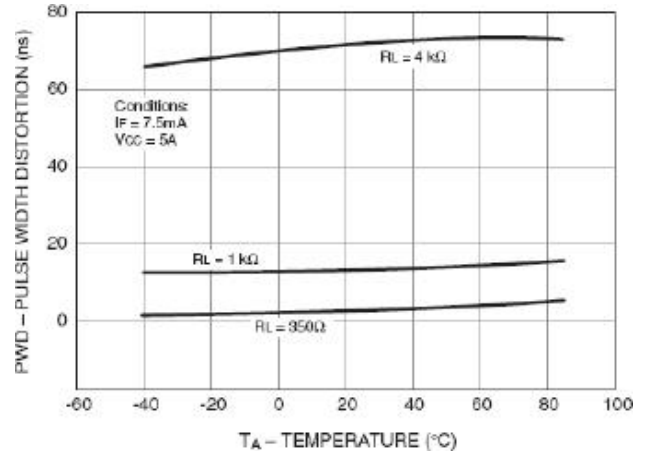


Fig.8 Pulse Width Distortion VS Temperature

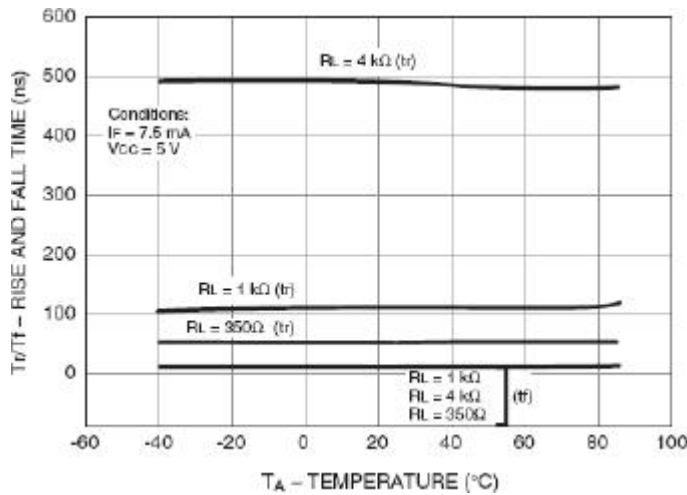


Fig.9 Rise and Fall Time VS Temperature

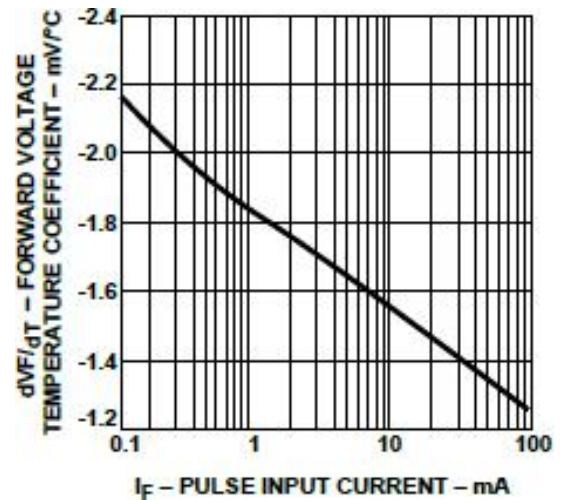


Fig.10 Temperature Coefficient for Forward Voltage VS. Input Current.

Test Circuits

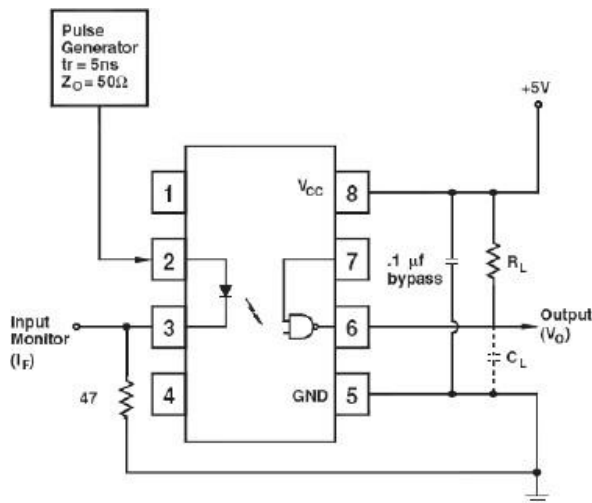


Fig.11 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f

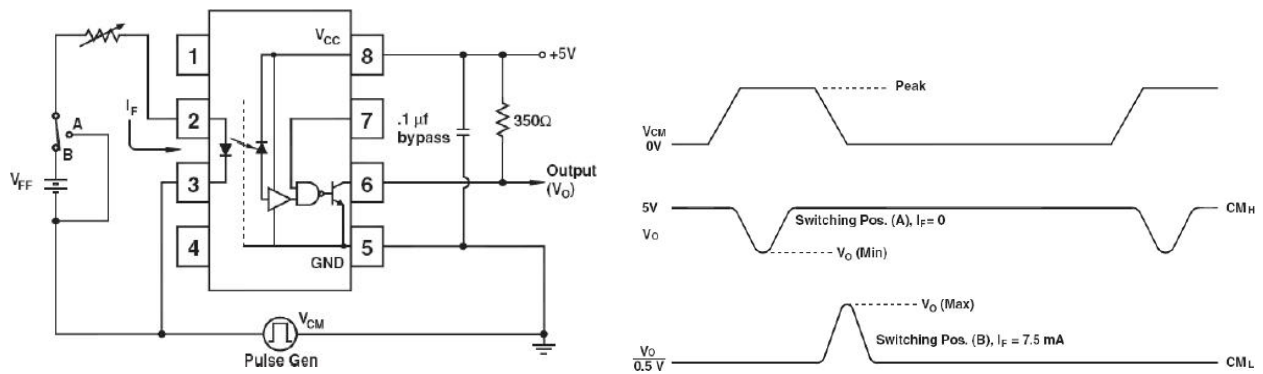
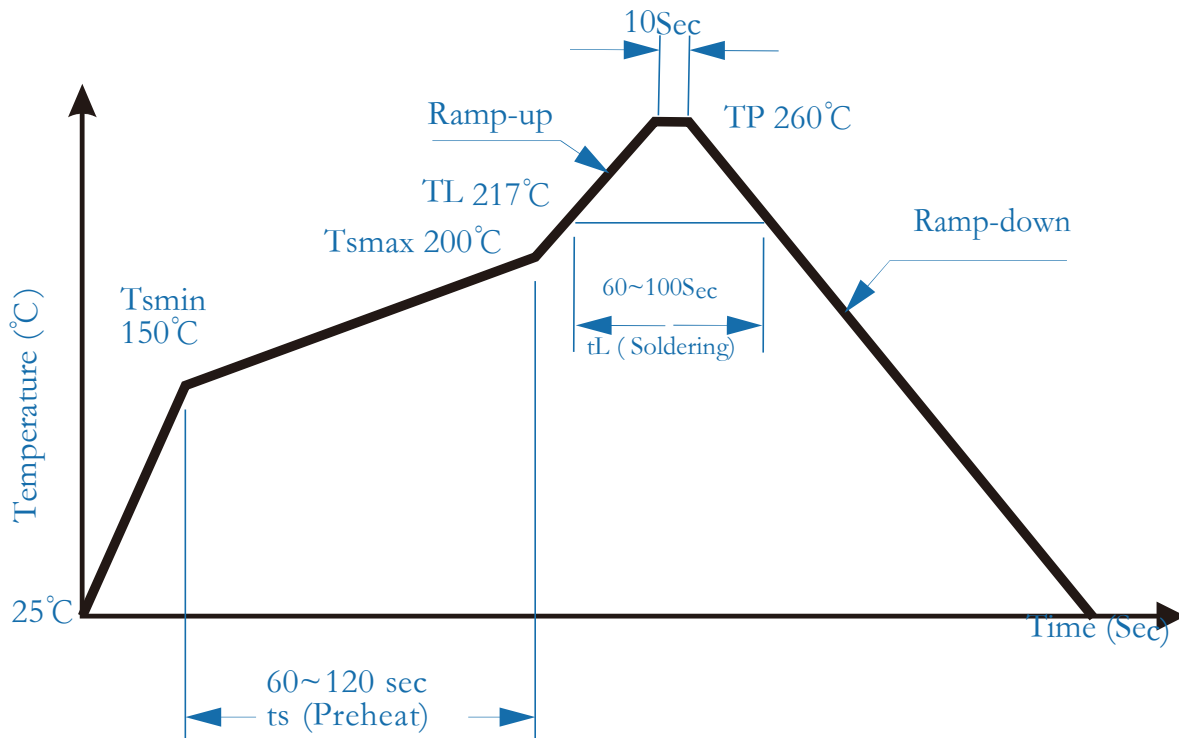


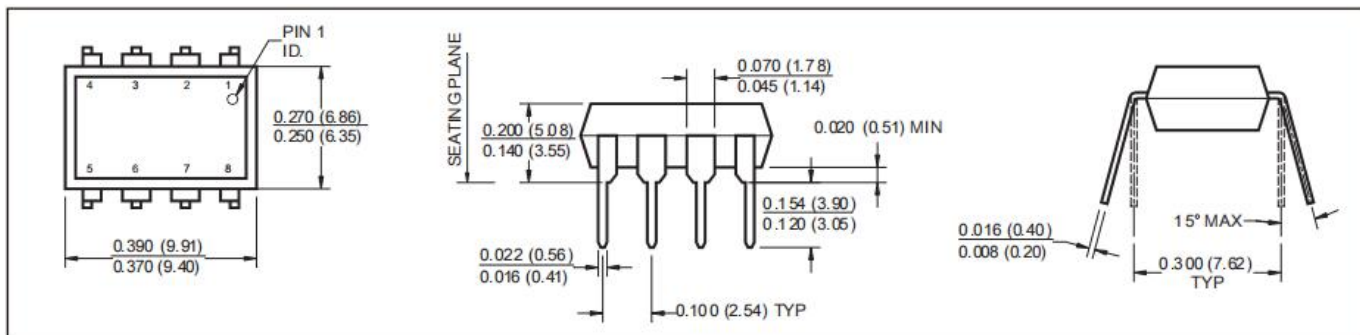
Fig. 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Solder Reflow Profile

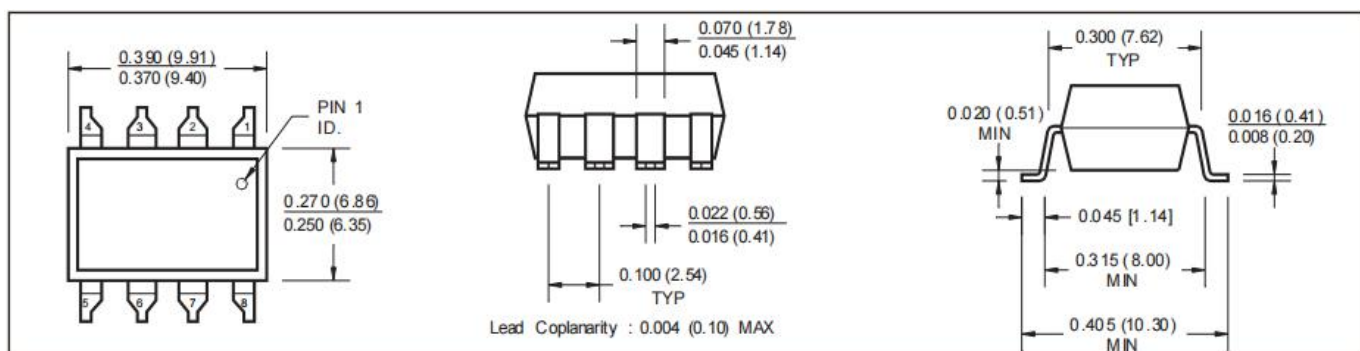


Package Dimensions

1. DIP



2. SMD



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