

LMx24, LMx24x, LMx24xx, LM2902, LM2902x, LM2902xx, LM2902xxx Quadruple Operational Amplifiers

1 Features

- Next-generation LM324B and LM2902B
- B versions are drop-in replacements for all versions of LM224, LM324, and LM2902
- Improved specifications of B version
 - Supply range: 3V to 36V (B, BA versions)
 - Low input offset voltage: $\pm 2\text{mV}$ (BA version) / 3mV (B version)
 - ESD rating: 2kV (HBM), 1.5kV (CDM)
 - EMI rejection: integrated RF and EMI filter
 - Low input bias current: 50nA maximum (across -40°C to 125°C)
- Common-mode input voltage range includes V_{-}
- Input voltage differential can be driven up to supply voltage
- For dual B versions, see [LM358B](#) and [LM2904B](#)

2 Applications

- [Merchant network and server power supply units](#)
- [Multi-function printers](#)
- [Power supplies and mobile chargers](#)
- [Desktop PC and motherboard](#)
- [Indoor and outdoor air conditioners](#)
- [Washers, dryers, and refrigerators](#)
- [AC inverters, string inverters, central inverters, and voltage frequency drives](#)
- [Uninterruptible power supplies](#)

3 Description

The LM324B and LM2902B devices are the next-generation versions of the industry-standard operational amplifiers (op amps) LM324 and LM2902, which include four high-voltage (36V) op amps. These devices provide outstanding value for cost-sensitive applications,

with features including low offset (600 μV , typical), common-mode input range to ground, and high differential input voltage capability.

The LM324B and LM2902B are unity-gain stable and achieve a low offset voltage maximum of 3mV (2mV maximum for LM324BA and LM2902BA) and quiescent current of 240 μA per amplifier (typical). High ESD (2kV HBM and 1.5kV CDM) and integrated EMI and RF filters enable the LM324B and LM2902B devices to be used in the most rugged, environmentally challenging applications.

The LM324B and LM2902B can drop-in replace all versions of the LM224, LM324, and LM2902 devices.

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE ⁽²⁾
LM324B, LM324BA, LM2902B, LM2902BA, LM324xx, LM224xx, LM124, LM2902xxx	D (SOIC, 14)	8.65mm $\times$ 6mm
LM324B, LM324BA, LM2902B, LM2902BA, LM324xx, LM124, LM2902xxx	PW (TSSOP, 14)	5mm $\times$ 6.4mm
LM324xx, LM224xx, LM2902xxx	N (PDIP, 14)	19.3mm $\times$ 9.4mm
LM324, LM324A, LM324K, LM324KA, LM2902, LM2902K	NS (SOP, 14)	10.3mm $\times$ 7.8mm
LM324A, LM2902K	DB (SSOP, 14)	6.2mm $\times$ 7.8mm
LM124A	J (CDIP, 14)	19.56mm $\times$ 6.67mm
	W (CFP, 14)	9.21mm $\times$ 6.3mm
	FK (LCCC, 20)	8.89mm $\times$ 8.89mm
LM324B, LM2902B	RTE (WQFN, 16 ⁽³⁾)	3mm $\times$ 3mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.
- (3) This package is preview only.

Family Comparison

SPECIFICATION	LM324B LM324BA	LM2902B LM2902BA	LM324 LM324A	LM324K LM324KA	LM2902	LM2902K LM2902KV LM2902KAV	LM224 LM224A	LM224K LM224KA	LM124 LM124A	Units
Supply voltage	3 to 36	3 to 36	3 to 30	3 to 30	3 to 26	3 to 26 (K) 3 to 30 (KV, KAV)	3 to 30	3 to 30	3 to 30	V
Offset voltage (max, 25°C)	± 3 ± 2	± 3 ± 2	± 7 ± 3	± 7 ± 3	± 7	± 7 (K, KV) ± 2 (KAV)	± 5 ± 3	± 5 ± 3	± 5 ± 2	mV
Input bias current at 25°C (typ / max)	10 / 35	10 / 35	20 / 250 15 / 100	20 / 250 15 / 100	20 / 250	20 / 250	20 / 150 15 / 80	20 / 150 15 / 80	20 / 150 – / 50	nA
ESD (HBM)	2000	2000	500	2000	500	2000	500	2000	500	V
Operating ambient temperature	-40 to 85	-40 to 125	0 to 70	0 to 70	-40 to 125	-40 to 125	-25 to 85	-25 to 85	-55 to 125	$^{\circ}\text{C}$



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4 Pin Configuration and Functions

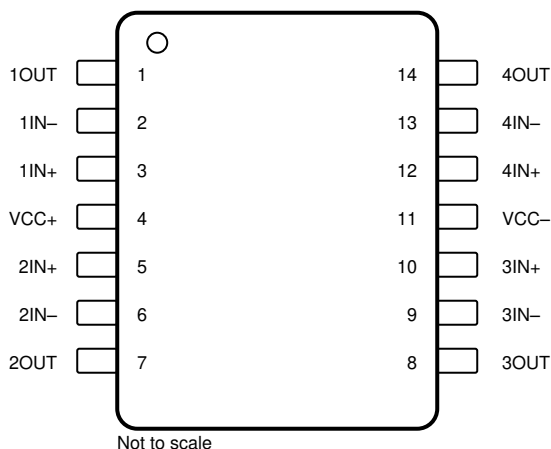


Figure 4-1. D, DB, J, N, NS, PW, and W Packages, 14-Pin SOIC, SSOP, CDIP, PDIP, SO, TSSOP, and CFP (Top View)

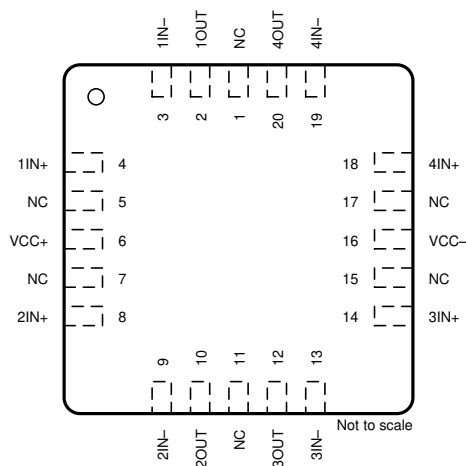
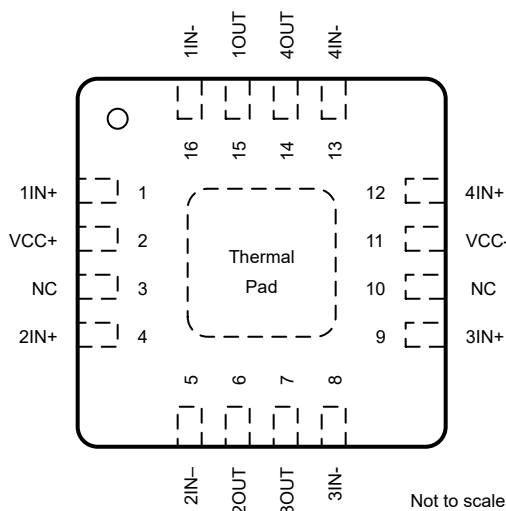


Figure 4-2. FK Package, 20-Pin LCCC (Top View)



NOTE: RTE package is preview only

Figure 4-3. RTE Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

NAME	PIN			TYPE ⁽¹⁾	DESCRIPTION
	LCCC	SOIC, TSSOP, PDIP, SSOP, SO, CDIP, and CFP	WQFN		
1IN-	3	2	16	I	Negative input
1IN+	4	3	1	I	Positive input
1OUT	2	1	15	O	Output
2IN-	9	6	5	I	Negative input
2IN+	8	5	4	I	Positive input

Table 4-1. Pin Functions (continued)

NAME	PIN			TYPE ⁽¹⁾	DESCRIPTION
	LCCC	SOIC, TSSOP, PDIP, SSOP, SO, CDIP, and CFP	WQFN		
2OUT	10	7	6	O	Output
3IN–	13	9	8	I	Negative input
3IN+	14	10	9	I	Positive input
3OUT	12	8	7	O	Output
4IN–	19	13	13	I	Negative input
4IN+	18	12	12	I	Positive input
4OUT	20	14	14	O	Output
V _{CC–}	16	11	11	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 5, 7, 11, 15, 17	—	3, 10	—	Do not connect
V _{CC+}	6	4	2	—	Positive (highest) supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	LM324B, LM324BA, LM2902B, LM2902BA		LM2902		LM324xx, LM224xx, LM2902xxx, LM124x		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC} ⁽²⁾		40		26		32	V
Differential input voltage, V_{ID} ⁽³⁾		±40		±26		±32	V
Input voltage, V_I (either input)	−0.3	40	−0.3	26	−0.3	32	V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_{CC} \leq 15\text{ V}$ ⁽⁴⁾	Unlimited		Unlimited		Unlimited		
Operating virtual junction temperature, T_J		150		150		150	°C
Case temperature for 60 seconds	FK package					260	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J or W package			300		300	°C
Storage temperature, T_{stg}	−65	150	−65	150	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at $IN+$, with respect to $IN-$.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.2 ESD Ratings

		VALUE	UNIT	
LM324B, LM324BA, LM2902B, LM2902BA, LM224K, LM224KA, LM324K, LM324KA, LM2902K, LM2902KV, LM2902KAV				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	
LM124, LM124A, LM224, LM224A, LM324, LM324A, LM2902				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	LM324B, LM324BA, LM2902B, LM2902BA		LM2902		LM324xx, LM224xx, LM2902xxx, LM124x		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	3	36	3	26	3	30	V
V_{CM} Common-mode voltage	0	$V_{CC} - 2$	0	$V_{CC} - 2$	0	$V_{CC} - 2$	V
T_A Operating free air temperature	LM124x				−55	125	°C
	LM2902xxx, LM2902Bx	−40	125	−40	125		
	LM324Bx	−40	85				
	LM224xx				−25	85	
	LM324xx				0	70	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMx24, LM2902						LMx24			UNIT
	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RTE (WQFN) (5)	FK (LCCC)	J (CDIP)	W (CFP)	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	16 PINS	20 PINS	14 PINS	14 PINS	
R _{θJA} ^{(2) (3)} Junction-to-ambient thermal resistance	99.3	106.5	83.5	90.4	124.7	64.9	74.5	84.7	153.4	°C/W
R _{θJC(top)} ⁽⁴⁾ Junction-to-case (top) thermal resistance	60.4	55.5	62.0	48.0	57.9	68.8	49.9	37.5	72.7	°C/W
R _{θJB}	57.5	56.8	57.7	49.2	80.7	40.2	49.0	72.2	146.5	
ψ _{JT}	19.8	18.2	40.5	14.4	8.4	4.9	42.9	31.0	48.3	
ψ _{JB}	57.0	55.8	57.1	48.8	79.8	40.0	48.9	67.3	129.2	
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	—	—	—	—	—	23.6	7.3	18.8	10.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
- (3) Maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/R_{θJA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_{J(max)} – T_C)/R_{θJC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) This package is preview only.

5.5 Electrical Characteristics - LM324B and LM324BA

For $V_S = (V+) - (V-) = 5\text{ V to }36\text{ V } (\pm 2.5\text{ V to } \pm 18\text{ V})$, at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE								
V _{OS}	Input offset voltage	LM324B			±0.6	±3.0	mV	
				T _A = −40°C to 85°C		±4.0		
		LM324BA			±0.3	±2		
				T _A = −40°C to 85°C		2.5		
dV _{OS} /dT	Input offset voltage drift	R _S = 0 Ω		T _A = −40°C to 85°C		±7	μV/°C	
PSRR	Input offset voltage versus power supply				65	100	dB	
	Channel separation	f = 1 kHz to 20 kHz				120	dB	
INPUT VOLTAGE RANGE								
V _{CM}	Common-mode voltage range	V _S = 3 V to 36 V			V−	(V+) − 1.5	V	
		V _S = 5 V to 36 V		T _A = −40°C to 85°C	V−	(V+) − 2		
CMRR	Common-mode rejection ratio	(V−) ≤ V _{CM} ≤ (V+) − 1.5 V	V _S = 3 V to 36 V	70	80		dB	
		(V−) ≤ V _{CM} ≤ (V+) − 2 V	V _S = 5 V to 36 V	T _A = −40°C to 85°C	65	80		
INPUT BIAS CURRENT								
I _B	Input bias current					−10	−35	nA
				T _A = −40°C to 85°C			−60	
dI _{OS} /dT	Input offset current drift				T _A = −40°C to 85°C	10	pA/°C	
I _{OS}	Input offset current					±0.5	±4	nA
				T _A = −40°C to 85°C			±5	
dI _{OS} /dT	Input offset current drift				T _A = −40°C to 85°C	10	pA/°C	
NOISE								
E _N	Input voltage noise	f = 0.1 to 10 Hz				3	μV _{PP}	
e _N	Input voltage noise density	R _S = 100 Ω, V _I = 0 V, f = 1 kHz (see Figure 7-2 for test circuit)				35	nV/√Hz	
INPUT CAPACITANCE								
Z _{ID}	Differential					10 0.1	MΩ pF	
Z _{ICM}	Common-mode					4 1.5	GΩ pF	
OPEN-LOOP GAIN								
A _{OL}	Open-loop voltage gain	V _S = 15 V, V _O = 1 V to 11 V, R _L ≥ 10 kΩ, connected to (V−)			50	100	V/mV	
					T _A = −40°C to 85°C	25		
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product	R _L = 1 MΩ, C _L = 20 pF (see Figure 7-1 for test circuit)				1.2	MHz	
SR	Slew rate	R _L = 1 MΩ, C _L = 30 pF, V _I = ±10 V (see Figure 7-1 for test circuit)				0.5	V/μs	
Θ _m	Phase margin	G = + 1, R _L = 10kΩ, C _L = 20 pF				56	°	
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V Step , G = +1, C _L = 100 pF				4	μs	
	Overload recovery time	V _{IN} × gain > V _S				10	μs	
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V _O = 3.53 V _{RMS} , V _S = 36 V, R _L = 100 kΩ, I _{OUT} ≤ 50 μA, BW = 80 kHz				0.001%		
OUTPUT								
V _O	Voltage output swing from rail	Positive Rail (V+)		I _{OUT} = −50 μA	1.35	1.5	V	
V _O				I _{OUT} = −1 mA	1.4	1.6	V	
V _O				I _{OUT} = −5 mA	1.5	1.75	V	
V _O		Negative Rail (V−)		I _{OUT} = 50 μA	100	150	mV	
V _O				I _{OUT} = 1 mA	0.75	1	V	
V _O				V _S = 5 V, R _L ≤ 10 kΩ connected to (V−)	T _A = −40°C to 85°C	5	20	mV
I _O	Output current	V _S = 15 V; V _O = V−; V _{ID} = 1 V	Source		−20 ⁽¹⁾	−30	mA	
				T _A = −40°C to 85°C	−10 ⁽¹⁾		mA	
		V _S = 15 V; V _O = V+; V _{ID} = −1 V	Sink		10 ⁽¹⁾	20	mA	
					T _A = −40°C to 85°C	5 ⁽¹⁾		mA
		V _{ID} = −1 V; V _O = (V−) + 200 mV			50	85	μA	
I _{SC}	Short-circuit current	V _S = 20 V, (V+) = 10 V, (V−) = −10 V, V _O = 0 V				±40	±60	mA
C _{LOAD}	Capacitive load drive					100		pF

5.5 Electrical Characteristics - LM324B and LM324BA (continued)

For $V_S = (V_+) - (V_-) = 5\text{ V to }36\text{ V}$ ($\pm 2.5\text{ V to } \pm 18\text{ V}$), at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R _O	Open-loop output impedance	f = 1 MHz, I _O = 0 A			300		Ω
POWER SUPPLY							
I _Q	Quiescent current per amplifier	V _S = 5 V; I _O = 0 A	T _A = −40°C to 85°C		240	300	μA
		V _S = 36 V; I _O = 0 A	T _A = −40°C to 85°C		350	750	μA

(1) Specified by design and characterization only.

5.6 Electrical Characteristics - LM2902B and LM2902BA

For $V_S = (V+) - (V-) = 5\text{ V to }36\text{ V}$ ($\pm 2.5\text{ V to } \pm 18\text{ V}$), at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM2902B			±0.6	±3.0	mV
			T _A = −40°C to 125°C			±4.0	
		LM2902BA			±0.3	±2	
			T _A = −40°C to 125°C			2.5	
dV _{OS} /dT	Input offset voltage drift	R _S = 0 Ω	T _A = −40°C to 125°C		±7		μV/°C
PSRR	Input offset voltage versus power supply			65	100		dB
	Channel separation	f = 1 kHz to 20 kHz			120		dB
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _S = 3 V to 36 V		V−	(V+) − 1.5		V
		V _S = 5 V to 36 V	T _A = −40°C to 125°C	V−	(V+) − 2		
CMRR	Common-mode rejection ratio	(V−) ≤ V _{CM} ≤ (V+) − 1.5 V	V _S = 3 V to 36 V	70	80		dB
		(V−) ≤ V _{CM} ≤ (V+) − 2 V	V _S = 5 V to 36 V	T _A = −40°C to 125°C	65	80	
INPUT BIAS CURRENT							
I _B	Input bias current				-10	-35	nA
			T _A = −40°C to 125°C			-60	
dI _{OS} /dT	Input offset current drift			T _A = −40°C to 125°C	10		pA/°C
I _{OS}	Input offset current				±0.5	±4	nA
			T _A = −40°C to 125°C			±5	
dI _{OS} /dT	Input offset current drift			T _A = −40°C to 125°C	10		pA/°C
NOISE							
E _N	Input voltage noise	f = 0.1 to 10 Hz			3		μV _{PP}
e _N	Input voltage noise density	R _S = 100 Ω, V _I = 0 V, f = 1 kHz (see Figure 7-2 for test circuit)			35		nV/√Hz
INPUT CAPACITANCE							
Z _{ID}	Differential				10 0.1		MΩ pF
Z _{ICM}	Common-mode				4 1.5		GΩ pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 15 V, V _O = 1 V to 11 V, R _L ≥ 10 kΩ, connected to (V−)			50	100	V/mV
				T _A = −40°C to 125°C	25		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	R _L = 1 MΩ, C _L = 20 pF (see Figure 7-1 for test circuit)			1.2		MHz
SR	Slew rate	R _L = 1 MΩ, C _L = 30 pF, V _I = ±10 V (see Figure 7-1 for test circuit)			0.5		V/μs
Θ _m	Phase margin	G = + 1, R _L = 10kΩ, C _L = 20 pF			56		°
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V Step , G = +1, C _L = 100 pF			4		μs
	Overload recovery time	V _{IN} × gain > V _S			10		μs
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V _O = 3.53 V _{RMS} , V _S = 36V, R _L = 100 kΩ, I _{OUT} ≤ 50 μA, BW = 80 kHz			0.001%		
OUTPUT							
V _O	Voltage output swing from rail	Positive Rail (V+)		I _{OUT} = -50 μA	1.35	1.5	V
V _O				I _{OUT} = -1 mA	1.4	1.6	V
V _O				I _{OUT} = -5 mA	1.5	1.75	V
V _O		Negative Rail (V-)		I _{OUT} = 50 μA	100	150	mV
V _O				I _{OUT} = 1 mA	0.75	1	V
V _O				V _S = 5 V, RL ≤ 10 kΩ connected to (V−)	T _A = −40°C to 125°C	5	20
I _O	Output current	V _S = 15 V; V _O = V−; V _{ID} = 1 V	Source		-20 ⁽¹⁾	-30	mA
				T _A = −40°C to 125°C	-10 ⁽¹⁾		mA
		V _S = 15 V; V _O = V+; V _{ID} = -1 V	Sink		10 ⁽¹⁾	20	mA
				T _A = −40°C to 125°C	5 ⁽¹⁾		mA
		V _{ID} = -1 V; V _O = (V−) + 200 mV			50	85	μA
I _{SC}	Short-circuit current	V _S = 20 V, (V+) = 10 V, (V−) = -10 V, V _O = 0 V			±40	±60	mA
C _{LOAD}	Capacitive load drive				100		pF

5.6 Electrical Characteristics - LM2902B and LM2902BA (continued)

For $V_S = (V_+) - (V_-) = 5\text{ V to }36\text{ V}$ ($\pm 2.5\text{ V to } \pm 18\text{ V}$), at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R _O	Open-loop output impedance	f = 1 MHz, I _O = 0 A			300		Ω
POWER SUPPLY							
I _Q	Quiescent current per amplifier	V _S = 5 V; I _O = 0 A	T _A = −40°C to 125°C		240	300	μA
		V _S = 36 V; I _O = 0 A	T _A = −40°C to 125°C			750	μA

(1) Specified by design and characterization only.

5.7 Electrical Characteristics for LM324, LM324K, LM224, LM224K, and LM124

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		T _A ⁽²⁾	LM124, LM224, LM224K			LM324, LM324K			UNIT		
					MIN	TYP ⁽³⁾	MAX	MIN	TYP ⁽³⁾	MAX			
V _{IO}	Input offset voltage	V _{CC} = 5 V to MAX, V _{IC} = V _{ICRmin} , V _O = 1.4 V		25°C	3			5	3			7	mV
				Full range			7			9			
I _{IO}	Input offset current	V _O = 1.4 V		25°C	2			30	2			50	nA
				Full range			100			150			
I _{IB}	Input bias current	V _O = 1.4 V		25°C	–20			–150	–20			–250	nA
				Full range			–300			–500			
V _{ICR}	Common-mode input voltage range	V _{CC} = 5 V to MAX		25°C	0 to V _{CC} – 1.5			0 to V _{CC} – 1.5			V		
				Full range			0 to V _{CC} – 2			0 to V _{CC} – 2			
V _{OH}	High-level output voltage	R _L = 2 kΩ		25°C	V _{CC} – 1.5			V _{CC} – 1.5			V		
		V _{CC} = MAX	R _L = 2 kΩ	Full range	26			26					
			R _L ≥ 10 kΩ	Full range	27	28	27			28			
V _{OL}	Low-level output voltage	R _L ≤ 10 kΩ		Full range	5			20	5			20	mV
A _{VD}	Large-signal differential voltage amplification	V _{CC+} = 15 V, V _O = 1 V to 11 V, R _L ≥ 2 kΩ		25°C	50	100	25			100	V/mV		
				Full range			25			15			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}		25°C	70	80	65			80	dB		
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})			25°C	65	100	65			100	dB		
V _{O1} / V _{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C	120			120			dB		
I _O	Output current	V _{CC} = 15 V, V _{ID} = 1 V, V _O = 0	Source	25°C	–20	–30	–60	–20	–30	–60	mA		
				Full range			–10						
		V _{CC} = 15 V, V _{ID} = –1 V, V _O = 15 V	Sink	25°C	10	20	10			20			
				Full range			5						
				V _{ID} = –1 V, V _O = 200 mV		25°C	12	30	12			30	μA
I _{OS}	Short-circuit output current	V _{CC} at 5 V, V _O = 0, V _{CC-} at –5 V		25°C	±40			±60	±40			±60	mA
I _{CC}	Supply current (four amplifiers)	V _O = 2.5 V, no load		Full range	0.7			1.2	0.7			1.2	mA
		V _{CC} = MAX, V _O = 0.5 V _{CC} , no load		Full range	1.4			3	1.4			3	

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 26 V for LM2902 and 30 V for the others.
- (2) Full range is –55°C to +125°C for LM124, –25°C to +85°C for LM224, and 0°C to 70°C for LM324.
- (3) All typical values are at $T_A = 25^\circ\text{C}$.

5.8 Electrical Characteristics for LM2902, LM2902K, LM2902KV and LM2902KAV

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		T _A ⁽²⁾	LM2902, LM2902K			LM2902KV, LM2902KAV			UNIT	
					MIN	TYP ⁽³⁾	MAX	MIN	TYP ⁽³⁾	MAX		
V _{IO}	Input offset voltage	V _{CC} = 5 V to MAX, V _{IC} = V _{ICRmin} , V _O = 1.4 V	Non-A-suffix devices	25°C		3	7		3	7	mV	
				Full range			10			10		
		A-suffix devices	25°C					1	2			
			Full range						4			
ΔV _{IO} /ΔT	Input offset voltage temperature drift	R _S = 0 Ω		Full range					7	μV/°C		
I _{IO}	Input offset current	V _O = 1.4 V		25°C		2	50		2	50	nA	
				Full range			300			150		
ΔI _{IO} /ΔT	Input offset voltage temperature drift			Full range					10	pA/°C		
I _{IB}	Input bias current	V _O = 1.4 V		25°C		–20	–250		–20	–250	nA	
				Full range			–500			–500		
V _{ICR}	Common-mode input voltage range	V _{CC} = 5 V to MAX		25°C		0 to V _{CC} – 1.5			0 to V _{CC} – 1.5	V		
				Full range		0 to V _{CC} – 2			0 to V _{CC} – 2			
V _{OH}	High-level output voltage	R _L = 10 kΩ		25°C		V _{CC} – 1.5			V _{CC} – 1.5		V	
		V _{CC} = MAX	R _L = 2 kΩ	Full range		22			26			
			R _L ≥ 10 kΩ	Full range		23	24		27			
V _{OL}	Low-level output voltage	R _L ≤ 10 kΩ		Full range		5	20		5	20	mV	
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 15 V, V _O = 1 V to 11 V, R _L ≥ 2 kΩ		25°C		25	100		25	100	V/mV	
				Full range		15			15			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}		25°C		50	80		60	80	dB	
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})			25°C		50	100		60	100	dB	
V _{O1} / V _{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120			120		dB	
I _O	Output current	V _{CC} = 15 V, V _{ID} = 1 V, V _O = 0	Source	25°C		–20	–30	–60	–20	–30	–60	mA
				Full range		–10			–10			
		V _{CC} = 15 V, V _{ID} = –1 V, V _O = 15 V	Sink	25°C		10	20		10	20		
				Full range		5			5			
		V _{ID} = –1 V, V _O = 200 mV		25°C		30			12	40		
I _{OS}	Short-circuit output current	V _{CC} at 5 V, V _O = 0, V _{CC} - at –5 V		25°C		±40	±60		±40	±60	mA	
I _{CC}	Supply current (four amplifiers)	V _O = 2.5 V, no load		Full range		0.7	1.2		0.7	1.2	mA	
		V _{CC} = MAX, V _O = 0.5 V _{CC} , no load		Full range		1.4	3		1.4	3		

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 26 V for LM2902 and 32 V for LM2902V.
- (2) Full range is -40°C to $+125^\circ\text{C}$ for LM2902.
- (3) All typical values are at $T_A = 25^\circ\text{C}$.

5.9 Electrical Characteristics for LM324A, LM324KA, LM224A, LM224KA, and LM124A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		T _A ⁽²⁾	LM124A			LM224A, LM224KA			LM324A, LM324KA			UNIT
					MIN	TYP ⁽³⁾	MAX	MIN	TYP ⁽³⁾	MAX	MIN	TYP ⁽³⁾	MAX	
V _{IO}	Input offset voltage	V _{CC} = 5 V to 30 V, V _{IC} = V _{ICRmin} , V _O = 1.4 V		25°C	2			2			3			mV
				Full range	4			4			5			
I _{IO}	Input offset current	V _O = 1.4 V		25°C	10			2			15			nA
				Full range	30			30			75			
I _{IB}	Input bias current	V _O = 1.4 V		25°C	−50			−15			−80			nA
				Full range	−100			−100			−200			
V _{ICR}	Common-mode input voltage range	V _{CC} = 30 V		25°C	0 to V _{CC} − 1.5			0 to V _{CC} − 1.5			0 to V _{CC} − 1.5			V
				Full range	0 to V _{CC} − 2			0 to V _{CC} − 2			0 to V _{CC} − 2			
V _{OH}	High-level output voltage	R _L = 2 kΩ		25°C	V _{CC} − 1.5			V _{CC} − 1.5			V _{CC} − 1.5			V
		V _{CC} = 30 V	R _L = 2 kΩ	Full range	26			26			26			
			R _L ≥ 10 kΩ	Full range	27			27 28			27 28			
V _{OL}	Low-level output voltage	R _L ≤ 10 kΩ		Full range	20			5 20			5 20			mV
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 15 V, V _O = 1 V to 11 V, R _L ≥ 2 kΩ		25°C	50	100	50 100			25 100			V/mV	
				Full range	25	25			15					
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}		25°C	70	70 80			65 80			dB		
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})			25°C	65	65 100			65 100			dB		
V _{O1} / V _{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C	120			120			120			dB
I _O	Output current	V _{CC} = 15 V, V _{ID} = 1 V, V _O = 0	Source	25°C	−20			−20 −30 −60			−20 −30 −60			mA
				Full range	−10			−10						
		V _{CC} = 15 V, V _{ID} = −1 V, V _O = 15 V	Sink	25°C	10			10 20			1 20			
				Full range	5			5			5			
		V _{ID} = −1 V, V _O = 200 mV	25°C	12			12 30			12 30			μA	
I _{OS}	Short-circuit output current	V _{CC} at 5 V, V _{CC} - at −5 V, V _O = 0		25°C	±40	±60	±40 ±60			±40 ±60			mA	
I _{CC}	Supply current (four amplifiers)	V _O = 2.5 V, no load		Full range	0.7	1.2	0.7 1.2			0.7 1.2			mA	
		V _{CC} = 30 V, V _O = 15 V, no load		Full range	1.4	3.	1.4 3			1.4 3				

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

(2) Full range is –55°C to +125°C for LM124A, –25°C to +85°C for LM224A, and 0°C to 70°C for LM324A.

(3) All typical values are at $T_A = 25^\circ\text{C}$.

5.10 Operating Conditions

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 30\text{ pF}$, $V_I = \pm 10\text{ V}$ (see Figure 6-1)	0.5	V/ μs
B_1 Unity-gain bandwidth	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$ (see Figure 6-1)	1.2	MHz
V_n Equivalent input noise voltage	$R_S = 100\text{ }\Omega$, $V_I = 0\text{ V}$, $f = 1\text{ kHz}$ (see Figure 6-2)	35	nV/ $\sqrt{\text{Hz}}$

5.11 Typical Characteristics

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

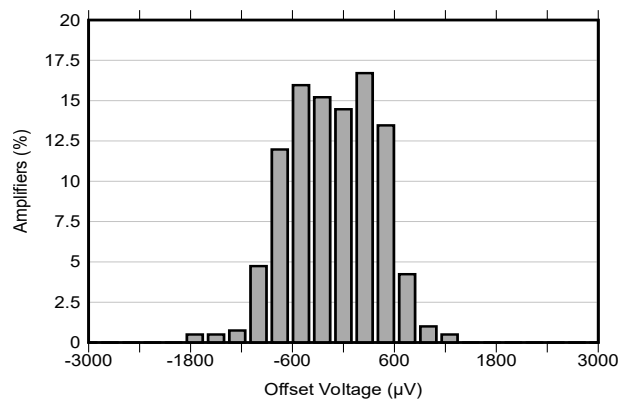


Figure 5-1. Offset Voltage Production Distribution

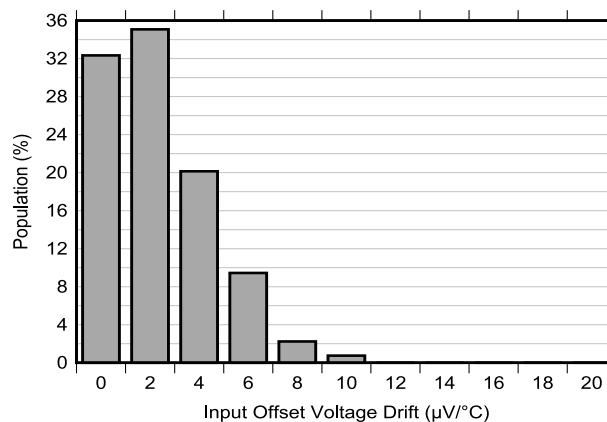


Figure 5-2. Offset Voltage Drift Distribution

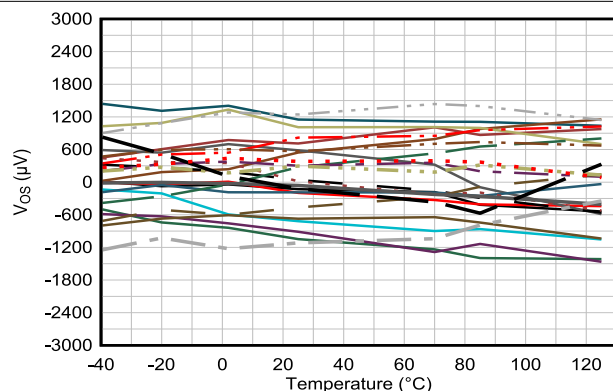


Figure 5-3. Offset Voltage vs Temperature

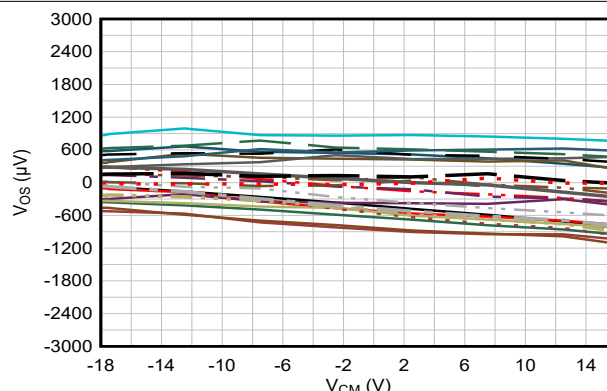


Figure 5-4. Offset Voltage vs Common-Mode Voltage

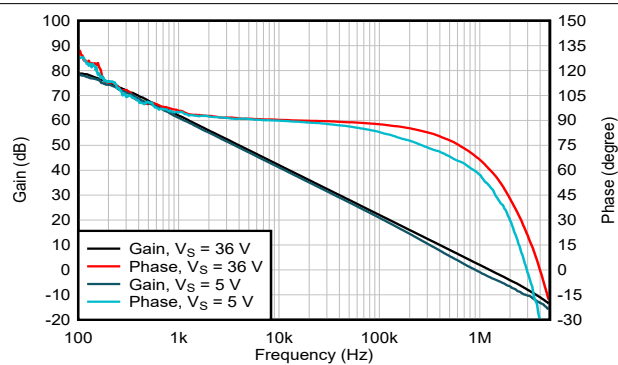


Figure 5-5. Open-Loop Gain and Phase vs Frequency

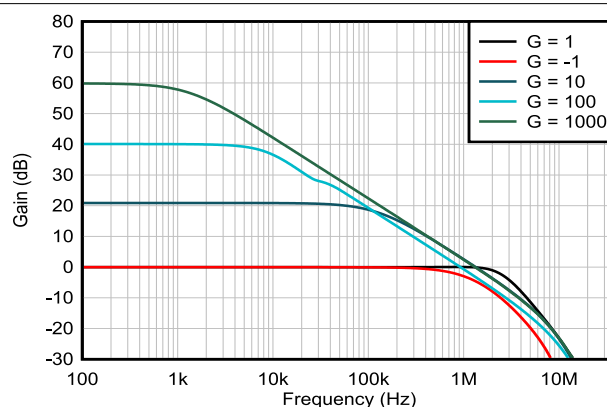


Figure 5-6. Closed-Loop Gain vs Frequency

5.11 Typical Characteristics (continued)

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

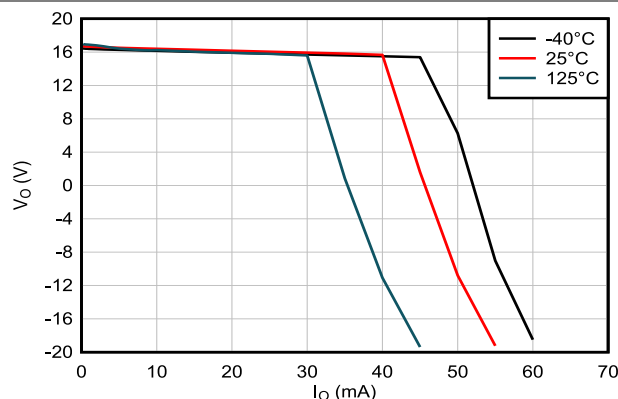


Figure 5-7. Output Voltage Swing vs Output Current (Sourcing)

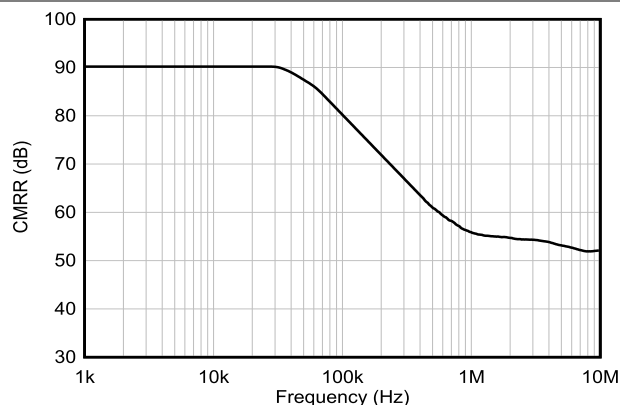


Figure 5-8. CMRR vs Frequency

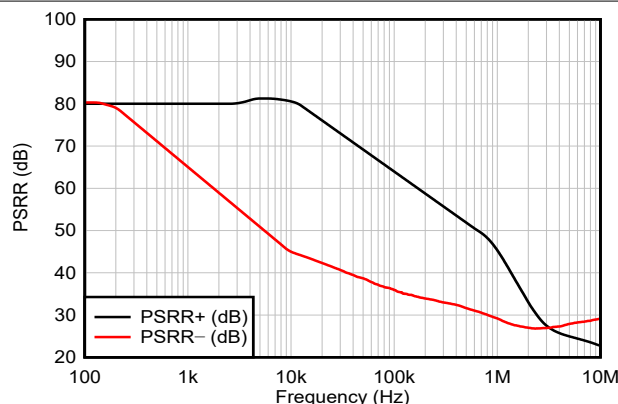


Figure 5-9. PSRR vs Frequency

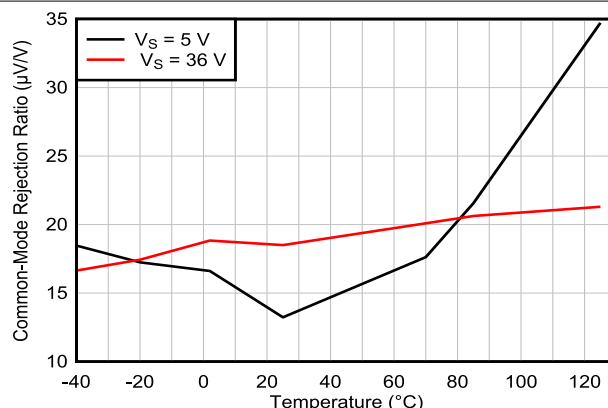


Figure 5-10. Common-Mode Rejection Ratio vs Temperature

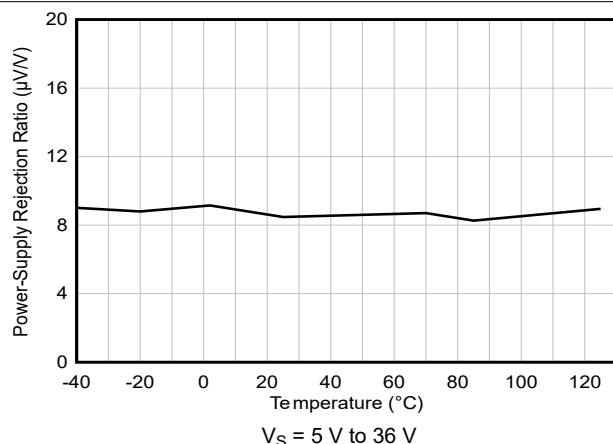


Figure 5-11. Power Supply Rejection Ratio vs Temperature

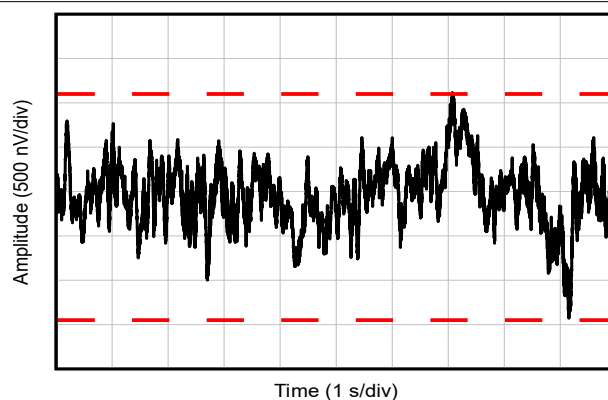


Figure 5-12. 0.1-Hz to 10-Hz Noise

5.11 Typical Characteristics (continued)

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

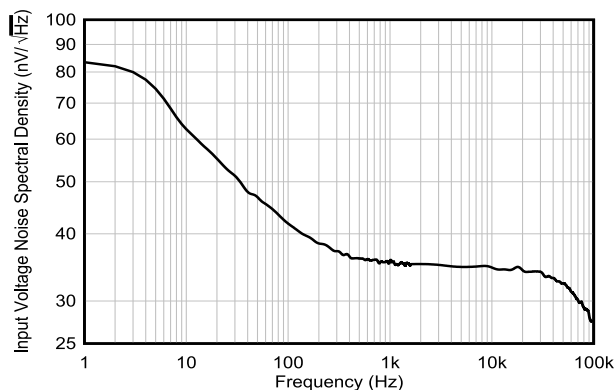


Figure 5-13. Input Voltage Noise Spectral Density vs Frequency

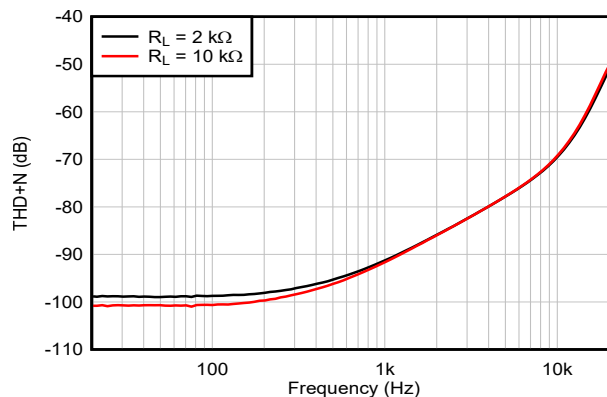


Figure 5-14. THD+N Ratio vs Frequency, $G = 1$

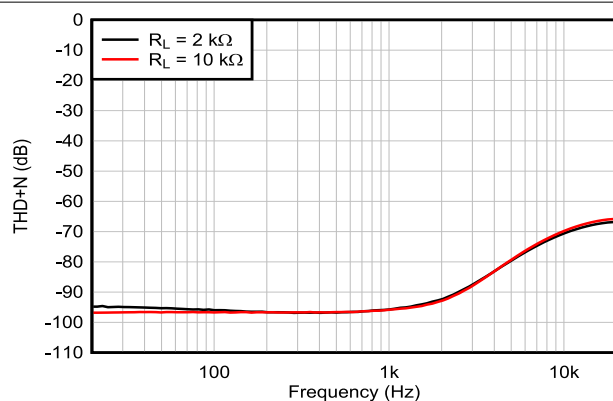


Figure 5-15. THD+N Ratio vs Frequency, $G = -1$

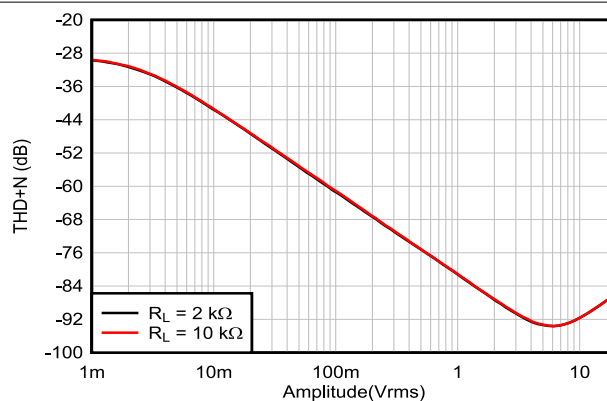


Figure 5-16. THD+N vs Output Amplitude, $G = 1$

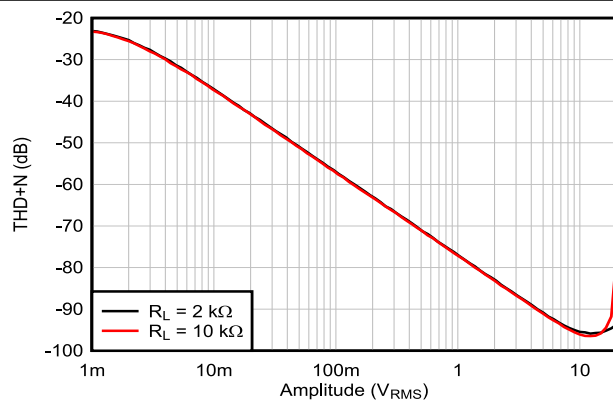


Figure 5-17. THD+N vs Output Amplitude, $G = -1$

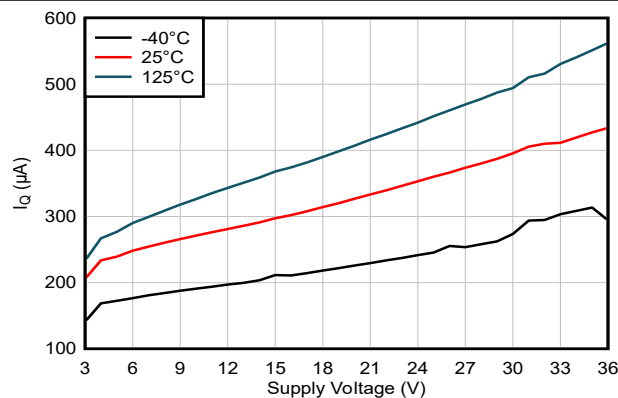


Figure 5-18. Quiescent Current vs Supply Voltage

5.11 Typical Characteristics (continued)

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

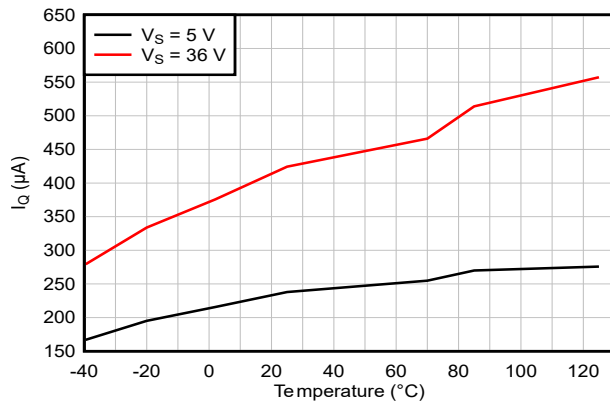


Figure 5-19. Quiescent Current vs Temperature

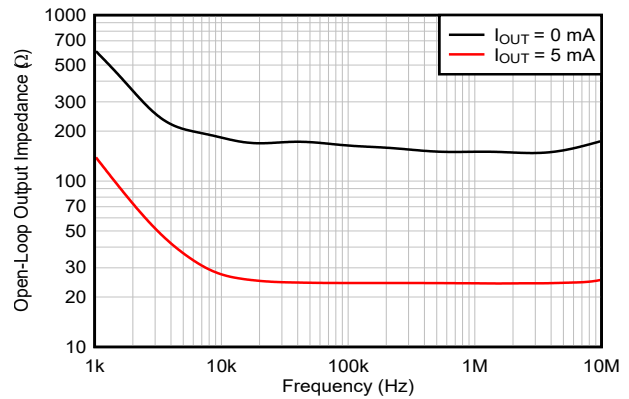
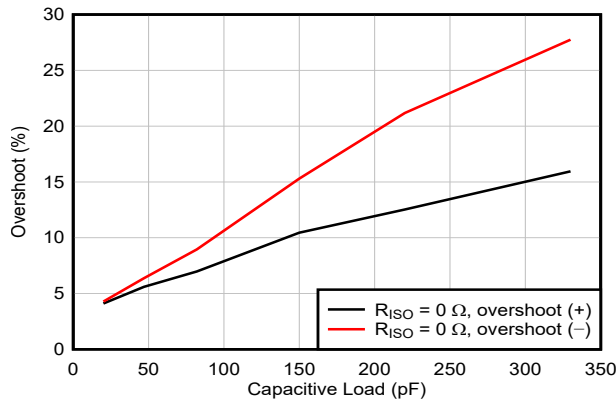
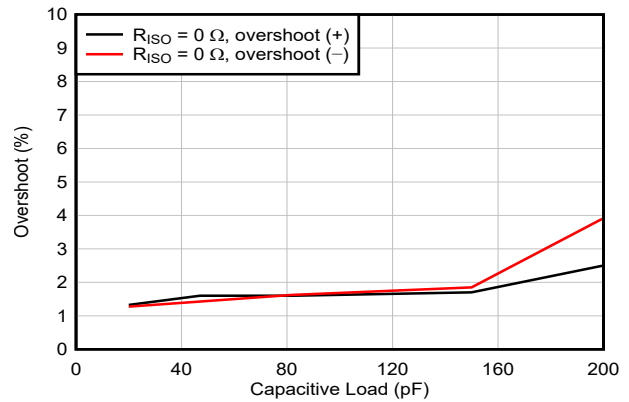


Figure 5-20. Open-Loop Output Impedance vs Frequency



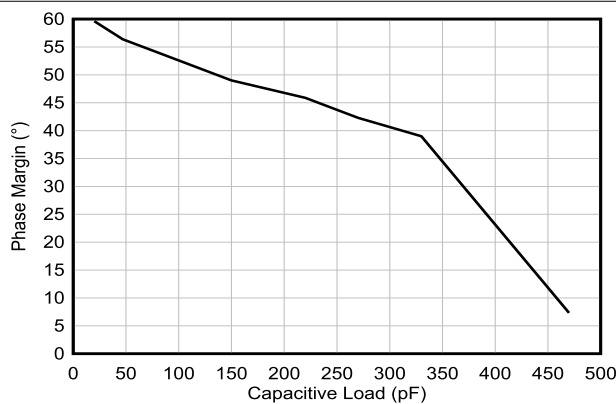
$G = 1$, 100-mV output step, R_L = open

Figure 5-21. Small-Signal Overshoot vs Capacitive Load



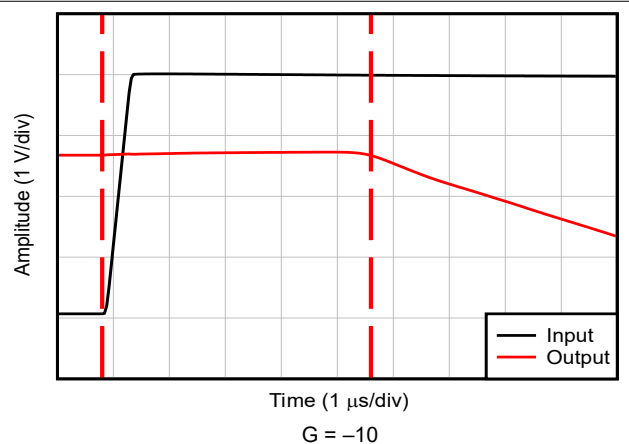
$G = -1$, 100-mV output step, R_L = open

Figure 5-22. Small-Signal Overshoot vs Capacitive Load



$G = +1$, $R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$

Figure 5-23. Phase Margin vs Capacitive Load



$G = -10$

Figure 5-24. Overload Recovery (Positive Rail)

5.11 Typical Characteristics (continued)

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

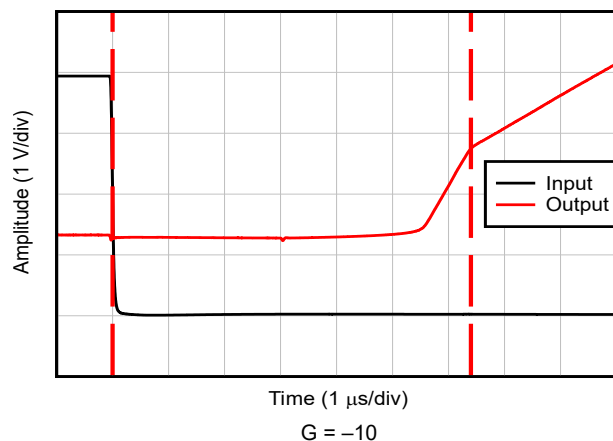


Figure 5-25. Overload Recovery (Negative Rail)

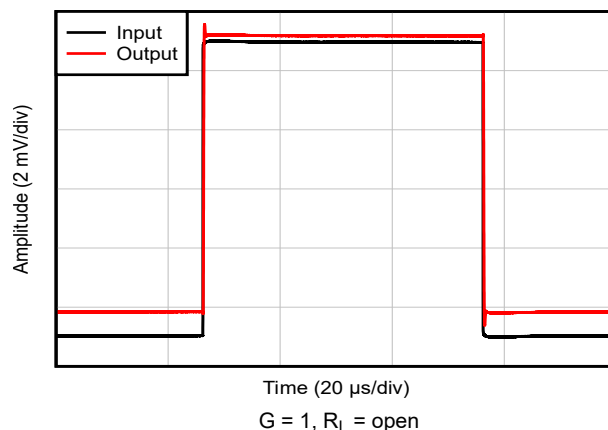


Figure 5-26. Small-Signal Step Response, $G = 1$

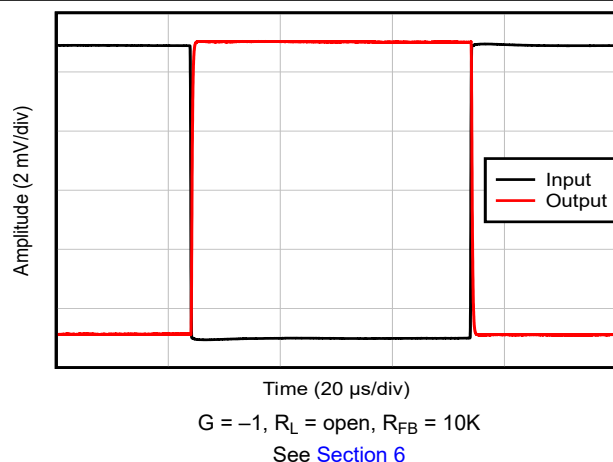


Figure 5-27. Small-Signal Step Response, $G = -1$

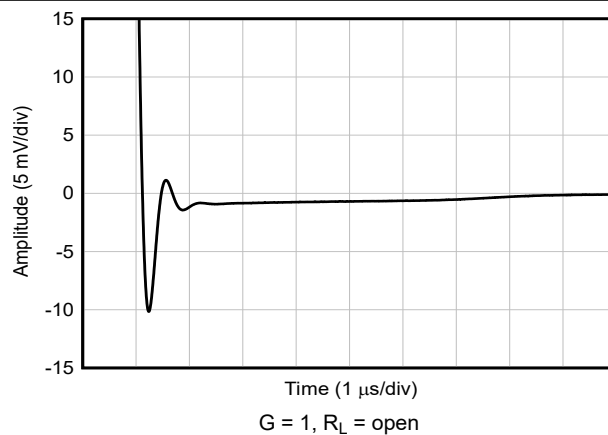


Figure 5-28. Large-Signal Step Response (Falling)

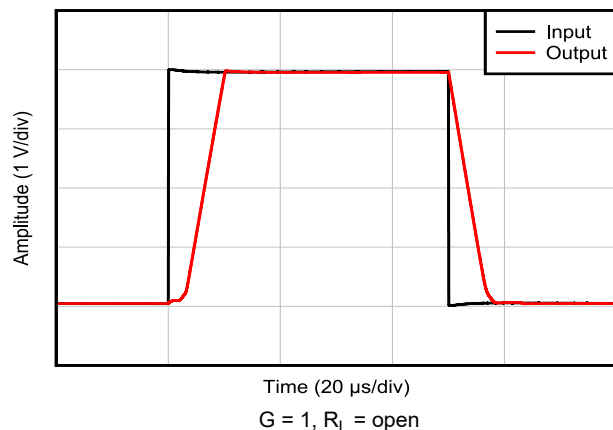


Figure 5-29. Large-Signal Step Response, $G = 1$

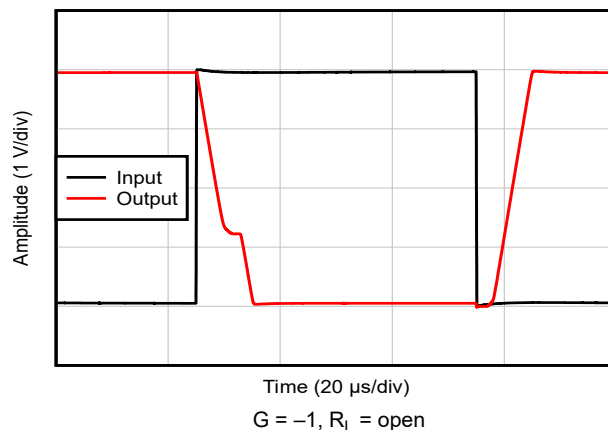


Figure 5-30. Large-Signal Step Response, $G = -1$

5.11 Typical Characteristics (continued)

This typical characteristics section is applicable for LM324B and LM2902B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

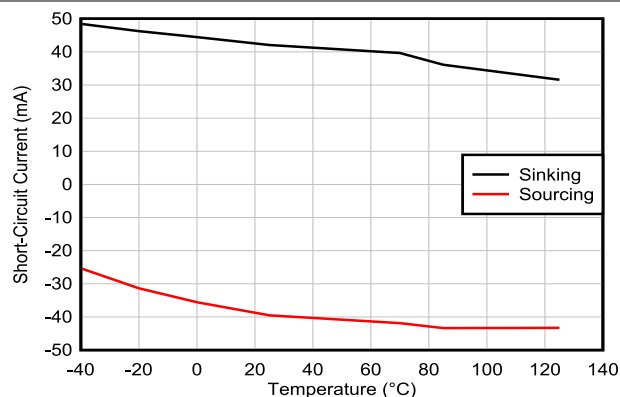


Figure 5-31. Short-Circuit Current vs Temperature

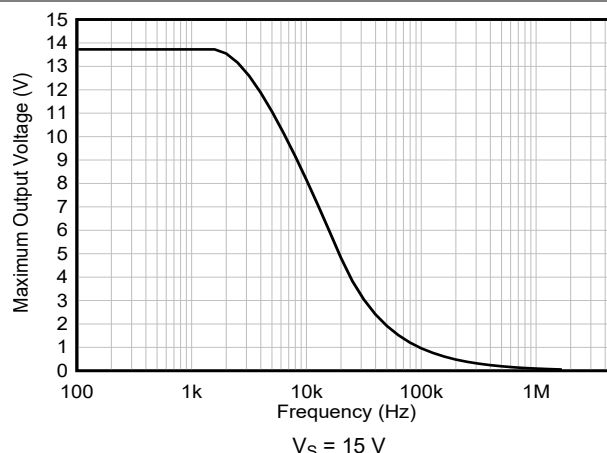


Figure 5-32. Maximum Output Voltage vs Frequency
 $V_S = 15\text{ V}$

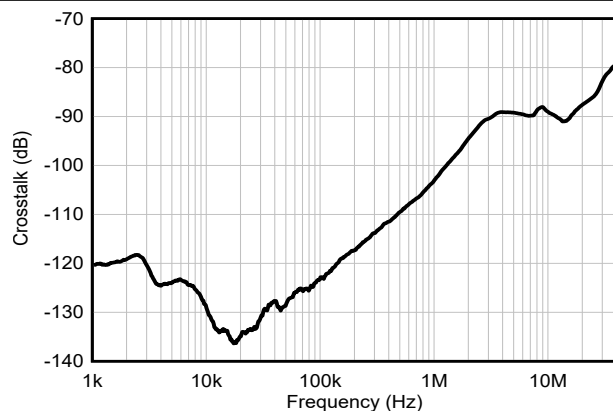


Figure 5-33. Channel Separation vs Frequency

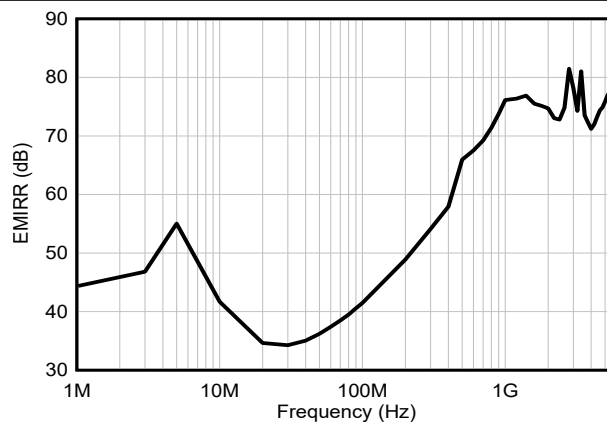


Figure 5-34. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

5.12 Typical Characteristics: All Devices Except B and BA Versions

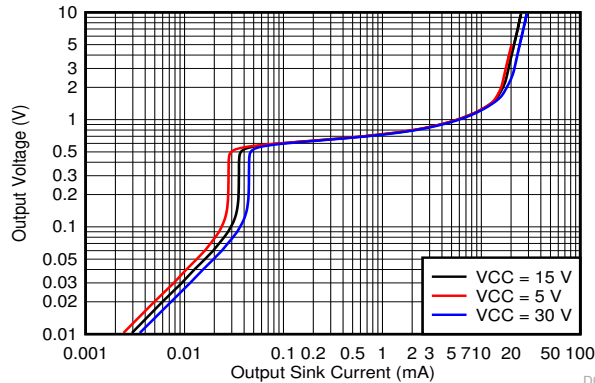


Figure 5-35. Output Sinking Characteristics

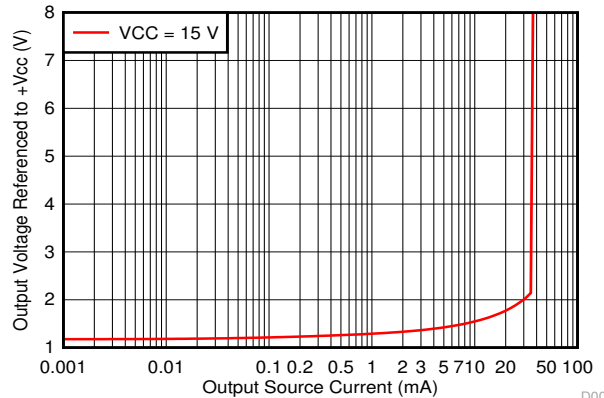


Figure 5-36. Output Sourcing Characteristics

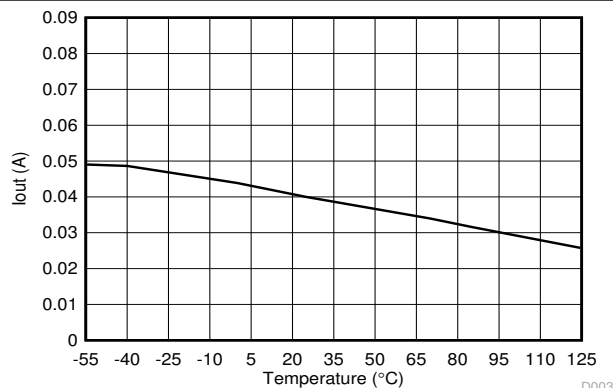


Figure 5-37. Source Current Limiting

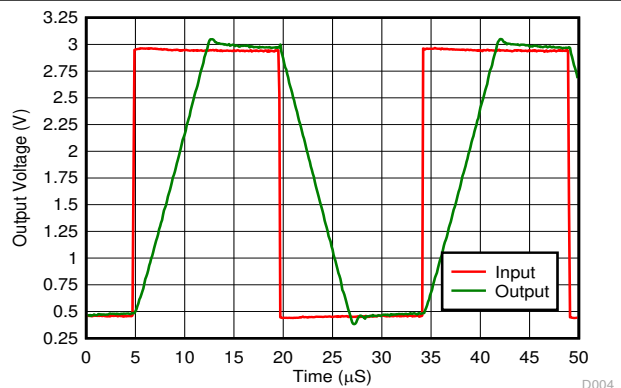


Figure 5-38. Voltage Follower Large Signal Response (50 pF)

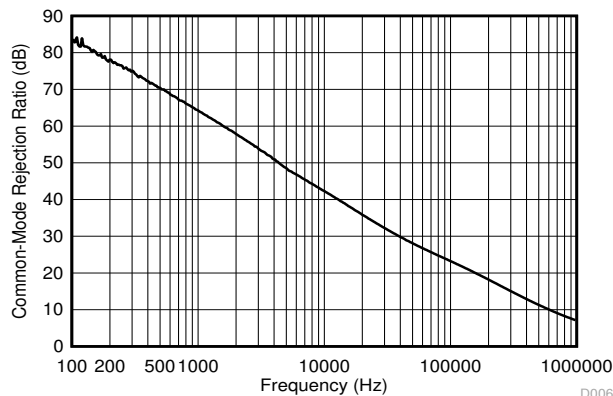


Figure 5-39. Common-Mode Rejection Ratio

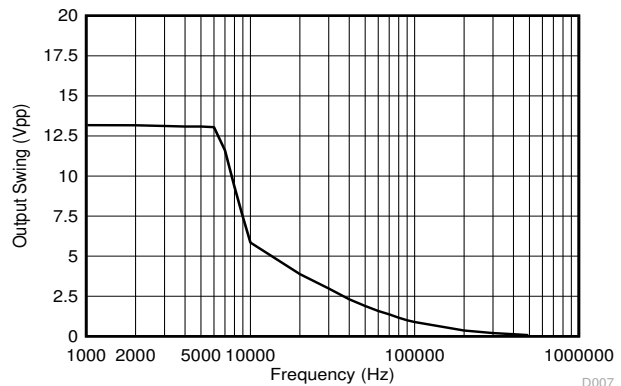


Figure 5-40. Maximum Output Swing vs. Frequency
(VCC = 15 V)

6 Parameter Measurement Information

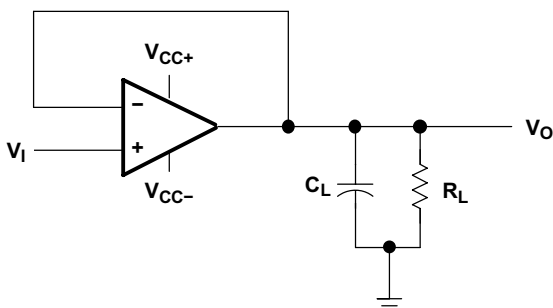


Figure 6-1. Unity-Gain Amplifier

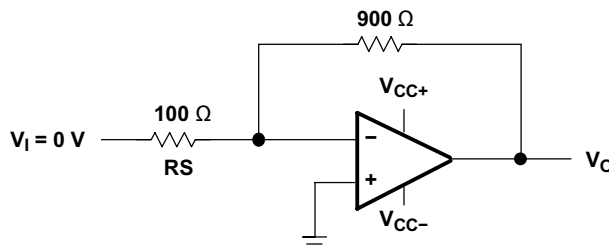


Figure 6-2. Noise-Test Circuit

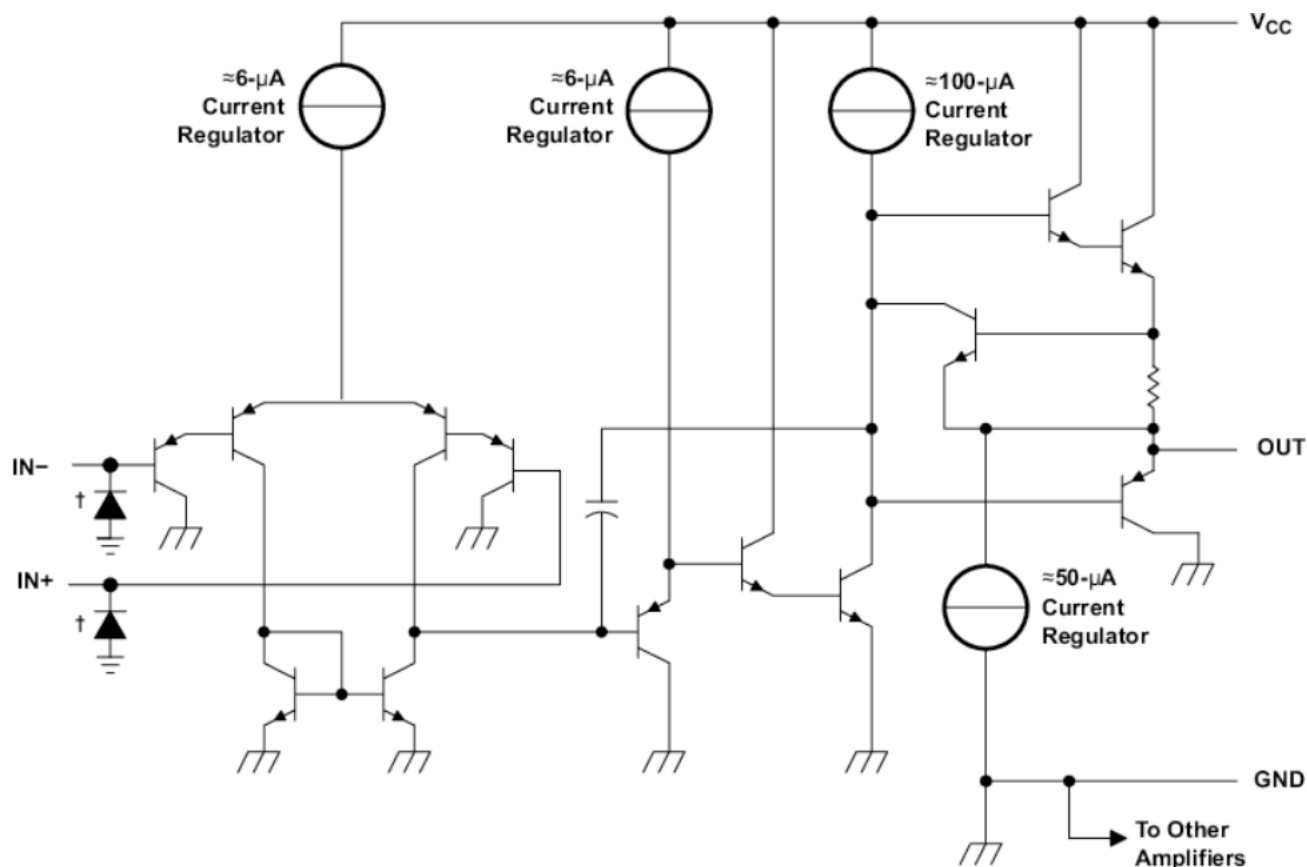
7 Detailed Description

7.1 Overview

These devices consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible if the difference between the two supplies is 3 V to 36 V (B and BA versions), 3 V to 26 V (for LM2902 devices), or 3 V to 30 V (for all other devices), and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that can be more easily implemented in single-supply-voltage systems. For example, the LM324B and LM2902B devices can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional ± 15 -V supplies.

7.2 Functional Block Diagram



COMPONENT COUNT (total device)	
Epi-FET	1
Transistors	95
Diodes	4
Resistors	11
Capacitors	4

ESD protection cells - available on B, BA, and K versions only

7.3 Feature Description

7.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate.

7.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_{CC} - 1.5\text{ V}$ ($V_{CC} - 2\text{ V}$ across temperature). Inputs may exceed V_{CC} up to the maximum V_{CC} without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range, then output phase is undefined. If either input is less than -0.3 V , then input current should be limited to 1 mA and output phase is undefined.

7.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMx24 and LM2902 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

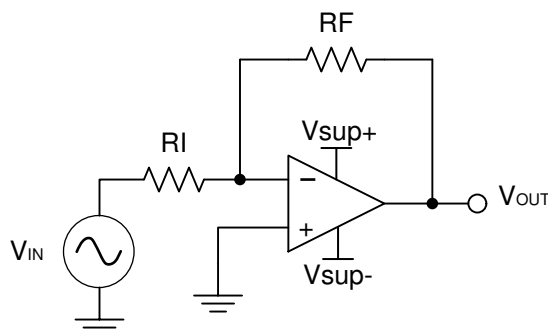


Figure 8-1. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the k Ω range is desirable because the amplifier circuit uses currents in the mA range. This choice makes sure that the part does not draw too much current. This example chooses 10 k Ω for R_I , which means 36 k Ω is used for R_F . This was determined by [Equation 3](#).

$$A_V = \frac{R_F}{R_I} \quad (3)$$

8.2.3 Application Curve

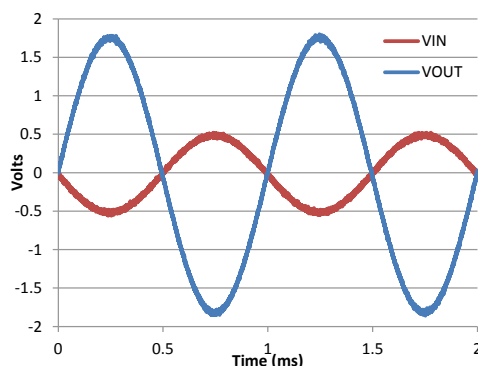


Figure 8-2. Input and Output Voltages of the Inverting Amplifier

8.3 Power Supply Recommendations

CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of ± 16 V for a dual supply can permanently damage the device (see the [Section 5.1](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Section 8.4](#).

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Section 8.4.2](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Examples

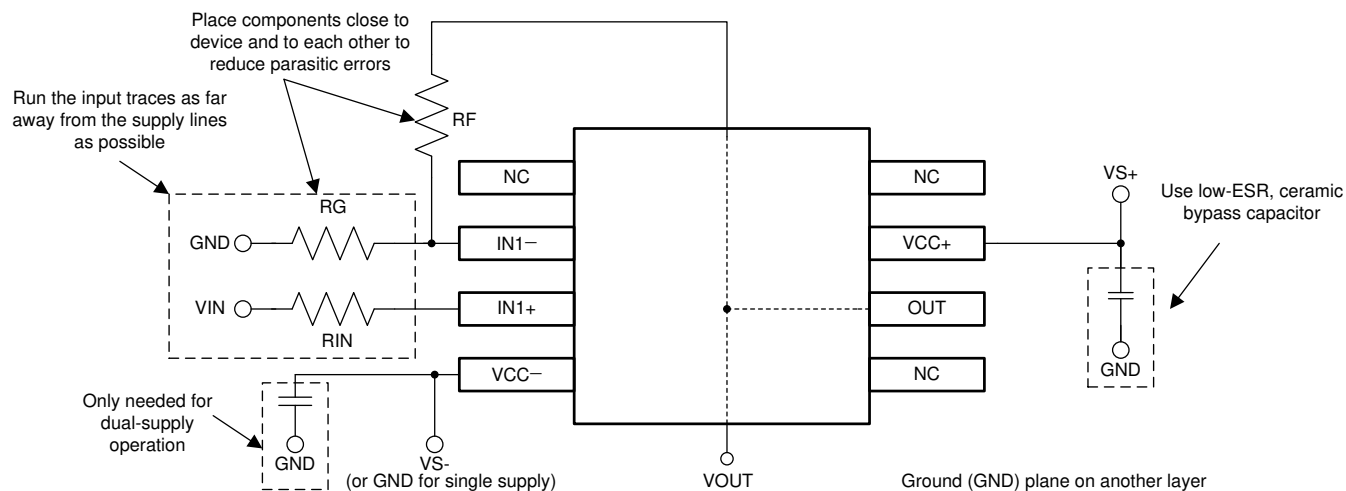


Figure 8-3. Operational Amplifier Board Layout for Noninverting Configuration

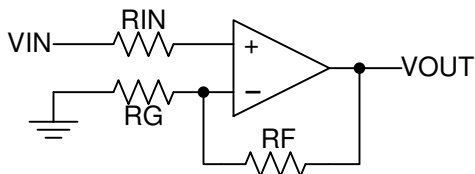


Figure 8-4. Operational Amplifier Schematic for Noninverting Configuration

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AC (March 2024) to Revision AD (October 2024) Page

- Removed the D (SOIC, 14) package preview note from the B and BA devices..... 1

Changes from Revision AB (November 2023) to Revision AC (March 2024) Page

- Added preview note to the WQFN-16 package pinout..... 3
- Added LM324BIRTER and LM2902BIRTER preview information to the *Mechanical, Packaging, and Orderable Information* section..... 28

Changes from Revision AA (September 2023) to Revision AB (November 2023) Page

- Changed the status of LM324BA and LM2902BA from: preview to: active..... 1

Changes from Revision Z (April 2023) to Revision AA (September 2023) Page

- Removed preview note from TSSOP-14 BA devices in *Device Information* table..... 1
- Changed the format of the *Package Information* table to include package lead size..... 1

Changes from Revision Y (October 2022) to Revision Z (April 2023)	Page
• Added WQFN-16 package in the <i>Package Information</i> table.....	1
• Added WQFN-16 package details to <i>Pin Configuration and Functions</i> section.....	3
• Added additional graphs for LM324Bx and LM2902Bx to <i>Typical Characteristics</i>	14

Changes from Revision X (May 2022) to Revision Y (October 2022)	Page
• Removed preview note from TSSOP-14 B devices in <i>Device Information</i> table.....	1
• Updated <i>Description</i> information.....	1
• Updated LM324B and LM324BA <i>Electrical Characteristics</i> table for RTM revision.....	7
• Updated LM2902B and LM2902BA <i>Electrical Characteristics</i> table for RTM revision.....	9
• Added graphs for LM324Bx and LM2902Bx to <i>Typical Characteristics</i>	14

Changes from Revision W (March 2015) to Revision X (May 2022)	Page
• Updated <i>Features</i> to include the B and BA versions.....	1
• Added application links to <i>Applications</i> section.....	1
• Corrected available packages in the <i>Device Information</i> table.....	1
• Added B and BA versions to <i>Device Information</i> table.....	1
• Updated package images in the <i>Pin Configuration and Functions</i> section to new format - no specification changes.....	3
• Renamed GND and Vcc to Vcc- and Vcc+, respectively, in the <i>Pin Functions</i> table	3
• Added B and BA versions to <i>Absolute Maximum Ratings</i> table	5
• Added the B and BA versions to the <i>ESD Ratings</i> table	5
• Added B and BA versions to <i>Recommended Operating Conditions</i> table	5
• Added the <i>Electrical Characteristics - LM324B and LM324BA</i> table	7
• Added the <i>Electrical Characteristics - LM2902B and LM2902BA</i> table.....	9
• Removed <i>Documentation Support</i> and <i>Related Links</i> in the <i>Device and Documentation Support</i> section.....	27

Changes from Revision V (January 2014) to Revision W (March 2014)	Page
• Added <i>Applications</i>	1
• Added <i>Device Information</i> table.....	1
• Added <i>Mechanical, Packaging, and Orderable Information</i> section.....	28

Changes from Revision U (August 2010) to Revision V (January 2014)	Page
• Updated document to new TI data sheet format - no specification changes.....	1
• Updated <i>Features</i>	1
• Updated <i>Features</i>	1
• Removed <i>Ordering Information</i> table.....	3
• Added <i>Pin Functions</i> table	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

11.1 Package Option Addendum

Packaging Information

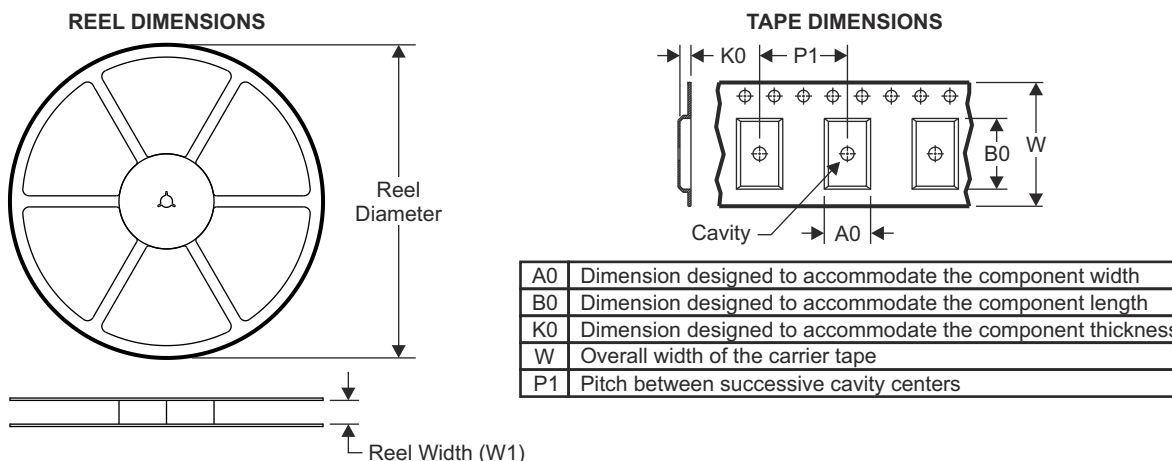
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
LM324BIRTER	PREVIEW	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM324B
LM2902BIRTER	PREVIEW	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902B

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

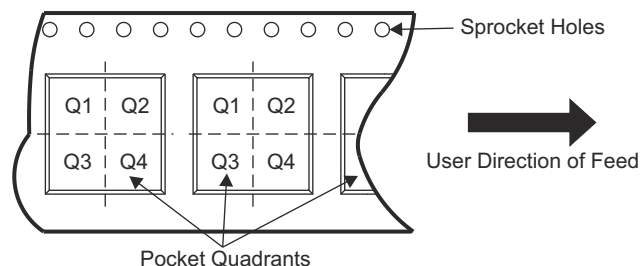
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

11.2 Tape and Reel Information

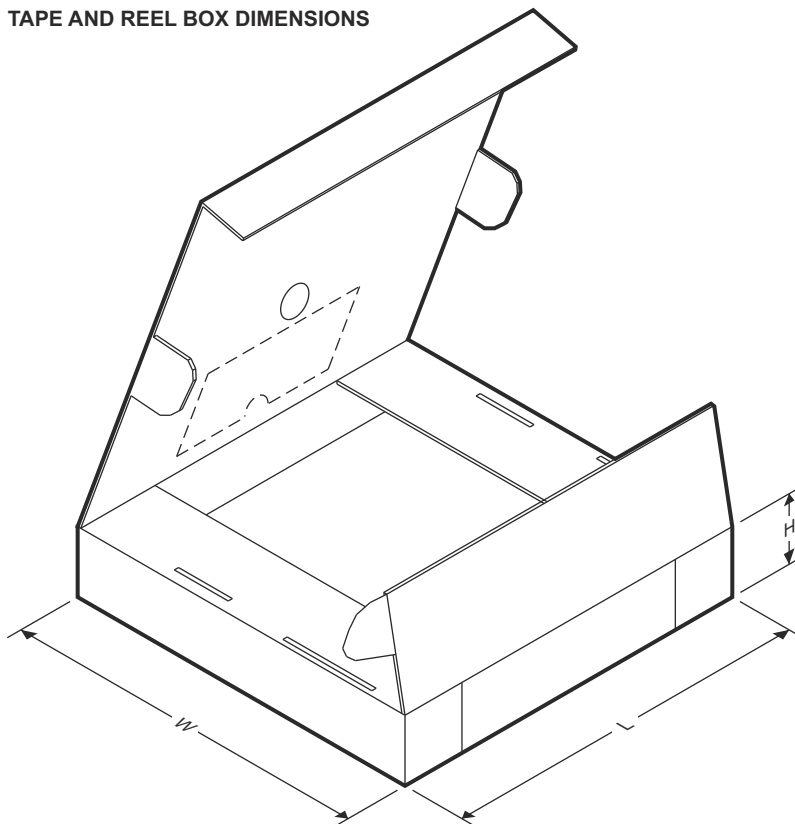


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM324BIRTER	WQFN	RTE	16	5000	330	12.4	3.3	3.3	1.1	8	12	Q2
LM2902BIRTER	WQFN	RTE	16	5000	330	12.4	3.3	3.3	1.1	8	12	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM324BIRTER	WQFN	RTE	16	5000	367.0	367.0	35.0
LM2902BIRTER	WQFN	RTE	16	5000	367.0	367.0	35.0

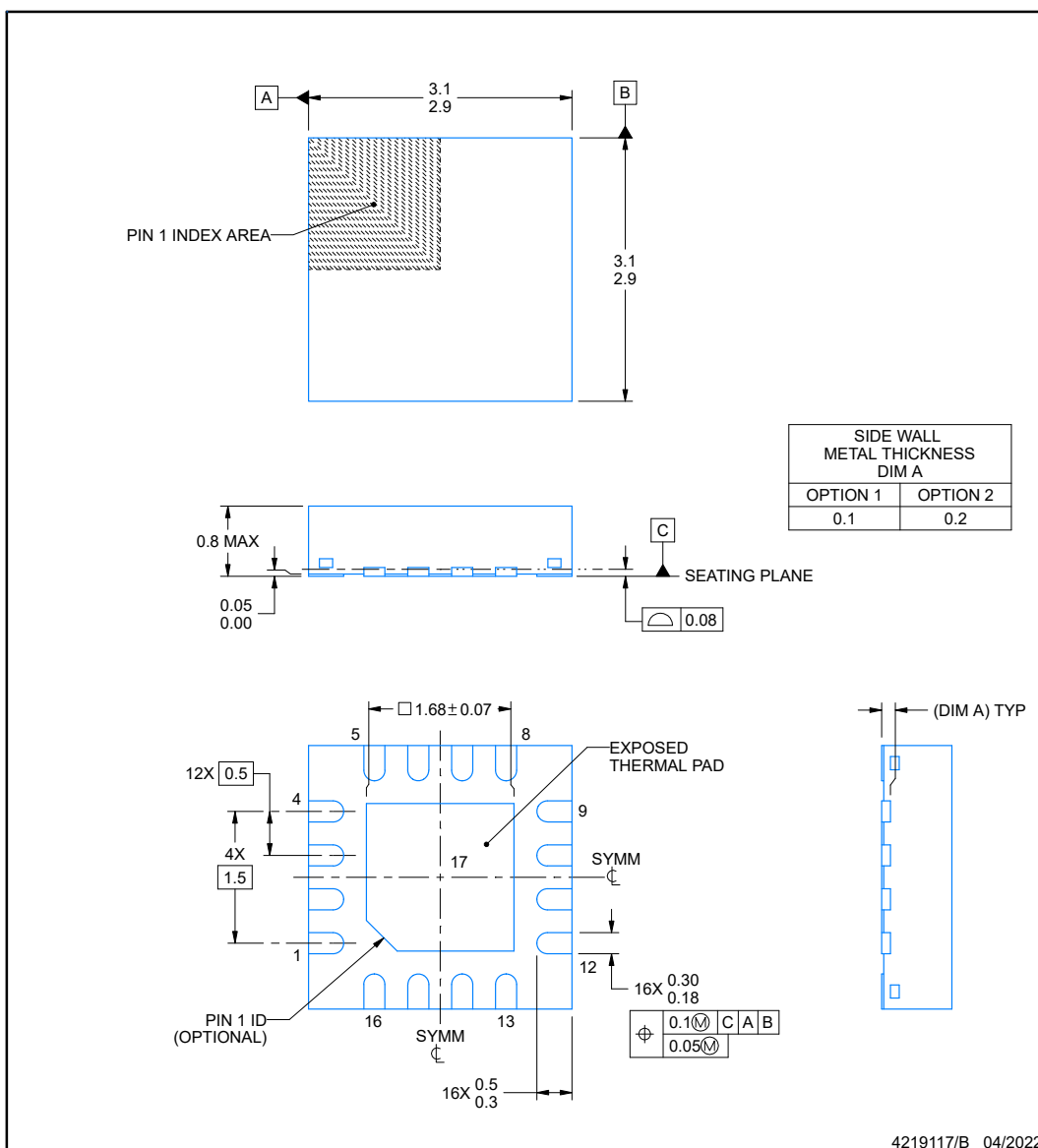


RTE0016C

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

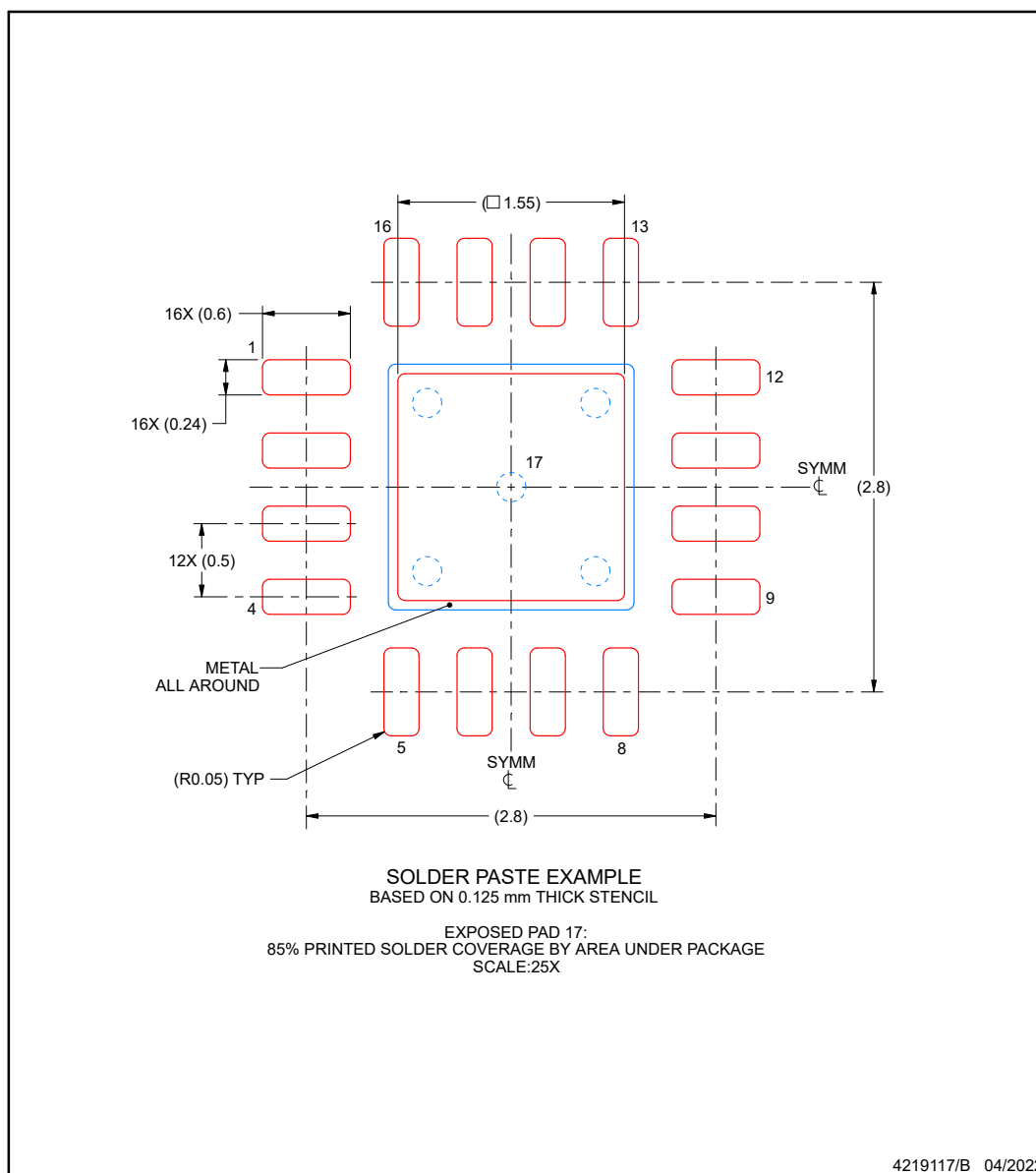
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7704301VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7704301VC A LM124JQMLV	Samples
5962-9950403V9B	ACTIVE	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962-9950403VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9950403VC A LM124AJQMLV	Samples
77043012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	Samples
7704301CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	Samples
7704301DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	Samples
77043022A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	Samples
7704302CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	Samples
7704302DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	Samples
JM38510/11005BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	Samples
LM124AFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	Samples
LM124AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124AJ	Samples
LM124AJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	Samples
LM124AWB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	Samples
LM124D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	LM124	
LM124DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Samples
LM124DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM124FKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	Samples
LM124J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124J	Samples
LM124JB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	Samples
LM124W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124W	Samples
LM124WB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	Samples
LM224AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM224A	
LM224ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	Samples
LM224AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224AN	Samples
LM224D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM224	
LM224DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224DRG3	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM224	
LM224DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	Samples
LM224KAD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-25 to 85	LM224KA	
LM224KADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	Samples
LM224KADRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-25 to 85		Samples
LM224KAN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KAN	Samples
LM224KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224K	Samples
LM224KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KN	Samples
LM224N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM224NE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	-25 to 85		Samples
LM2902BAIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902BA	Samples
LM2902BIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902B	Samples
LM2902D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LM2902	
LM2902DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LM2902	Samples
LM2902DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Samples
LM2902DRG3	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LM2902	
LM2902DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Samples
LM2902KAVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Samples
LM2902KAVQDRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	L2902KA	
LM2902KAVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Samples
LM2902KAVQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	Samples
LM2902KD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LM2902K	
LM2902KDB	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2902KN	Samples
LM2902KNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KNSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	Samples
LM2902KPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	L2902K	
LM2902KPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	Samples
LM2902KVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples
LM2902KVQDRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	L2902KV	
LM2902KVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2902KVQPWRG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	L2902KV	
LM2902N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-40 to 125	LM2902N	Samples
LM2902NE4	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 125	LM2902N	
LM2902NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	Samples
LM2902PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	L2902	
LM2902PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM2902PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM2902PWRG3	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	L2902	
LM2902PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	Samples
LM324AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM324A	
LM324ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ADRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM324A	
LM324AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324AN	Samples
LM324ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	Samples
LM324APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L324A	
LM324APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	Samples
LM324BAIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L324BA	Samples
LM324BIPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM324B	Samples
LM324D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM324	
LM324DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM324	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324DRG3	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM324	
LM324DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324KAD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LM324KA	
LM324KADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KADRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70		Samples
LM324KAN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324KAN	Samples
LM324KANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	Samples
LM324KAPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L324KA	
LM324KAPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	Samples
LM324KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	Samples
LM324KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324KN	Samples
LM324KNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	Samples
LM324KPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L324K	
LM324KPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324K	Samples
LM324N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM324N	Samples
LM324NE3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	LM324N	
LM324NE4	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	LM324N	
LM324NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324NSRE4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	Samples
LM324PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L324	
LM324PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L324	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	Samples
LM324PWRG3	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	L324	
LM324PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	Samples
M38510/11005BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	Samples
PLM2902BIDR	ACTIVE	SOIC	D	14	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLM324BIDR	ACTIVE	SOIC	D	14	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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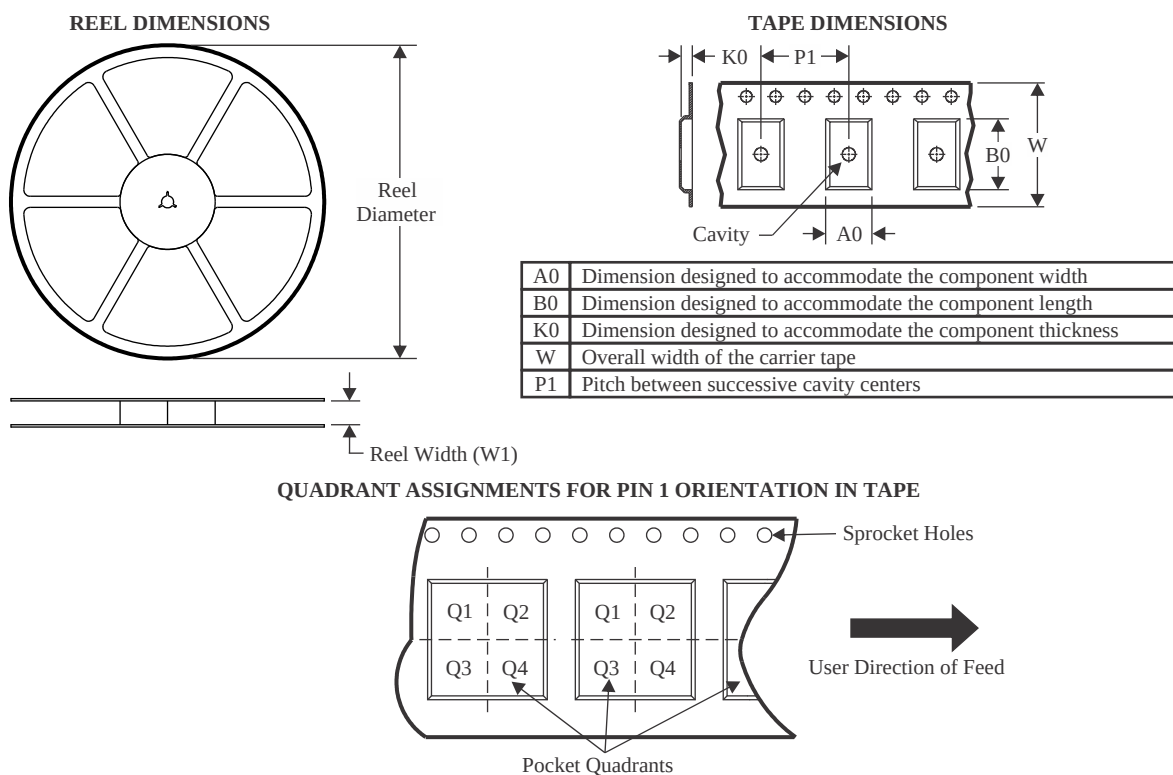
OTHER QUALIFIED VERSIONS OF LM124, LM124-SP, LM124M, LM2902, LM2902B, LM2902BA :

- Catalog : [LM124](#), [LM124](#)
- Automotive : [LM2902-Q1](#), [LM2902B-Q1](#), [LM2902BA-Q1](#)
- Enhanced Product : [LM2902-EP](#)
- Military : [LM124M](#), [LM124M](#)
- Space : [LM124-SP](#), [LM124-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

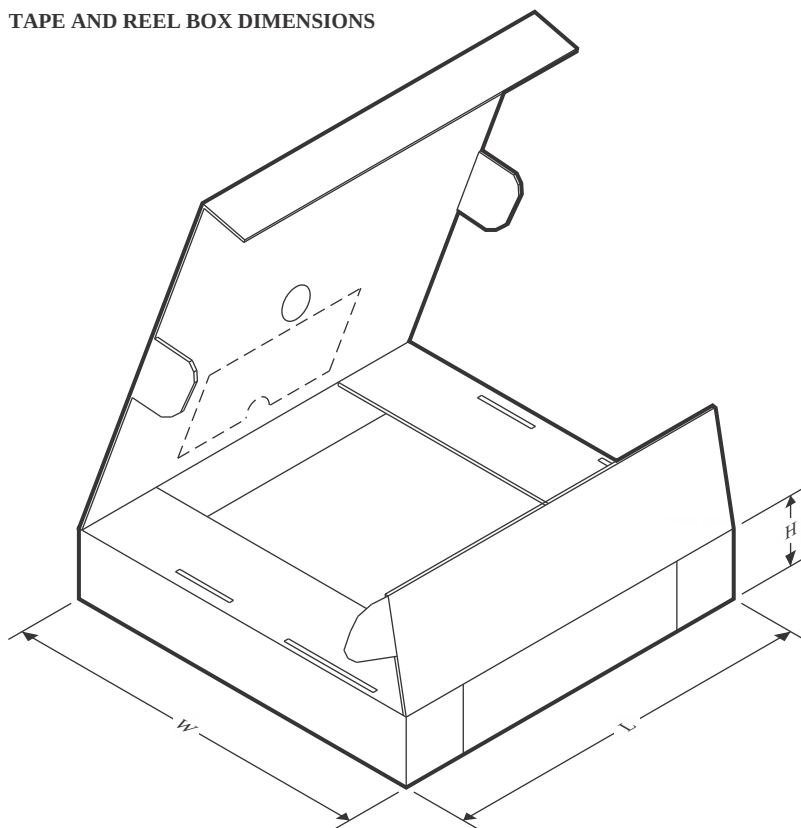


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM124DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902BAIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KAVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KAVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM324ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324BAIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324BIPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KAPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

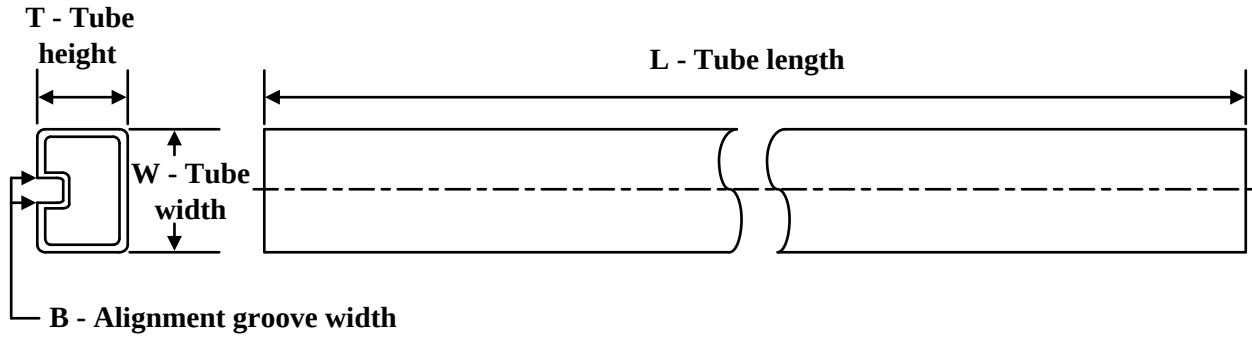
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM124DR	SOIC	D	14	2500	350.0	350.0	43.0
LM224ADR	SOIC	D	14	2500	340.5	336.1	32.0
LM224ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM224ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM224ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM224DR	SOIC	D	14	2500	356.0	356.0	35.0
LM224DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM224KADR	SOIC	D	14	2500	356.0	356.0	35.0
LM224KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM2902BAIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM2902BIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM2902DR	SOIC	D	14	2500	353.0	353.0	32.0
LM2902DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM2902KAVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902KAVQPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM2902KNSR	SO	NS	14	2000	356.0	356.0	35.0
LM2902KPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902KVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902NSR	SO	NS	14	2000	356.0	356.0	35.0
LM2902PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM324ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM324ANSR	SO	NS	14	2000	356.0	356.0	35.0
LM324APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324BAIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM324BIPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LM324DR	SOIC	D	14	2500	356.0	356.0	35.0
LM324DR	SOIC	D	14	2500	353.0	353.0	32.0
LM324DRG4	SOIC	D	14	2500	353.0	353.0	32.0
LM324DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM324KADR	SOIC	D	14	2500	356.0	356.0	35.0
LM324KANSR	SO	NS	14	2000	356.0	356.0	35.0
LM324KAPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM324KNSR	SO	NS	14	2000	356.0	356.0	35.0
LM324KPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324NSR	SO	NS	14	2000	356.0	356.0	35.0
LM324PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

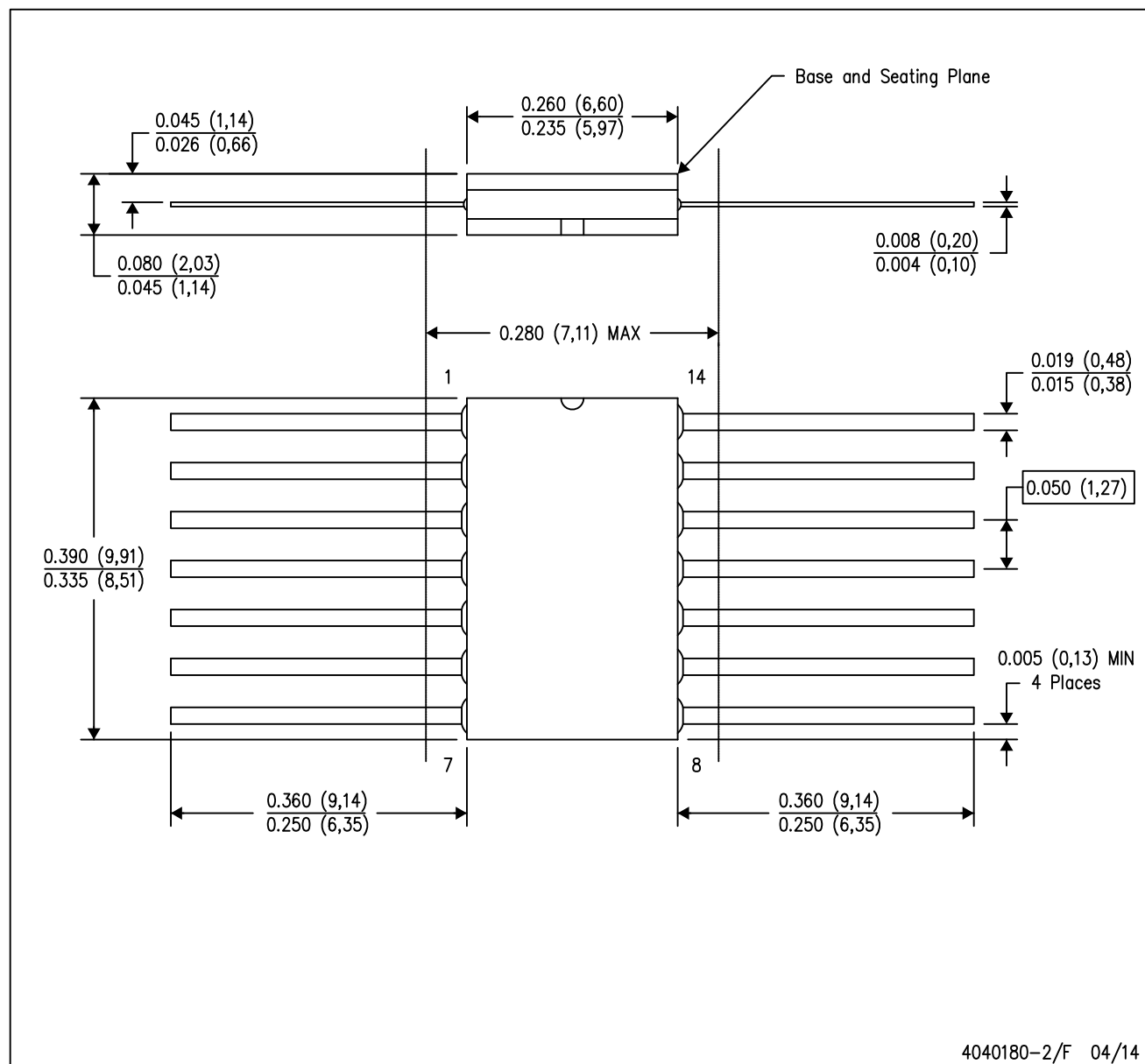
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9950403VCA	J	CDIP	14	25	506.98	15.24	13440	NA
77043012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7704301DA	W	CFP	14	25	506.98	26.16	6220	NA
77043022A	FK	LCCC	20	55	506.98	12.06	2030	NA
7704302DA	W	CFP	14	25	506.98	26.16	6220	NA
LM124AFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM124AWB	W	CFP	14	25	506.98	26.16	6220	NA
LM124FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM124W	W	CFP	14	25	506.98	26.16	6220	NA
LM124WB	W	CFP	14	25	506.98	26.16	6220	NA
LM224AN	N	PDIP	14	25	506	13.97	11230	4.32
LM224KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM224KN	N	PDIP	14	25	506	13.97	11230	4.32
LM224N	N	PDIP	14	25	506	13.97	11230	4.32
LM2902KDB	DB	SSOP	14	80	530	10.5	4000	4.1
LM2902KN	N	PDIP	14	25	506	13.97	11230	4.32
LM2902N	N	PDIP	14	25	506.1	9	600	5.4
LM2902N	N	PDIP	14	25	506	13.97	11230	4.32
LM324AN	N	PDIP	14	25	506	13.97	11230	4.32
LM324AN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KN	N	PDIP	14	25	506	13.97	11230	4.32
LM324N	N	PDIP	14	25	506.1	9	600	5.4
LM324N	N	PDIP	14	25	506	13.97	11230	4.32
LM324N	N	PDIP	14	25	506	13.97	11230	4.32
LM324N	N	PDIP	14	25	506	13.97	11230	4.32

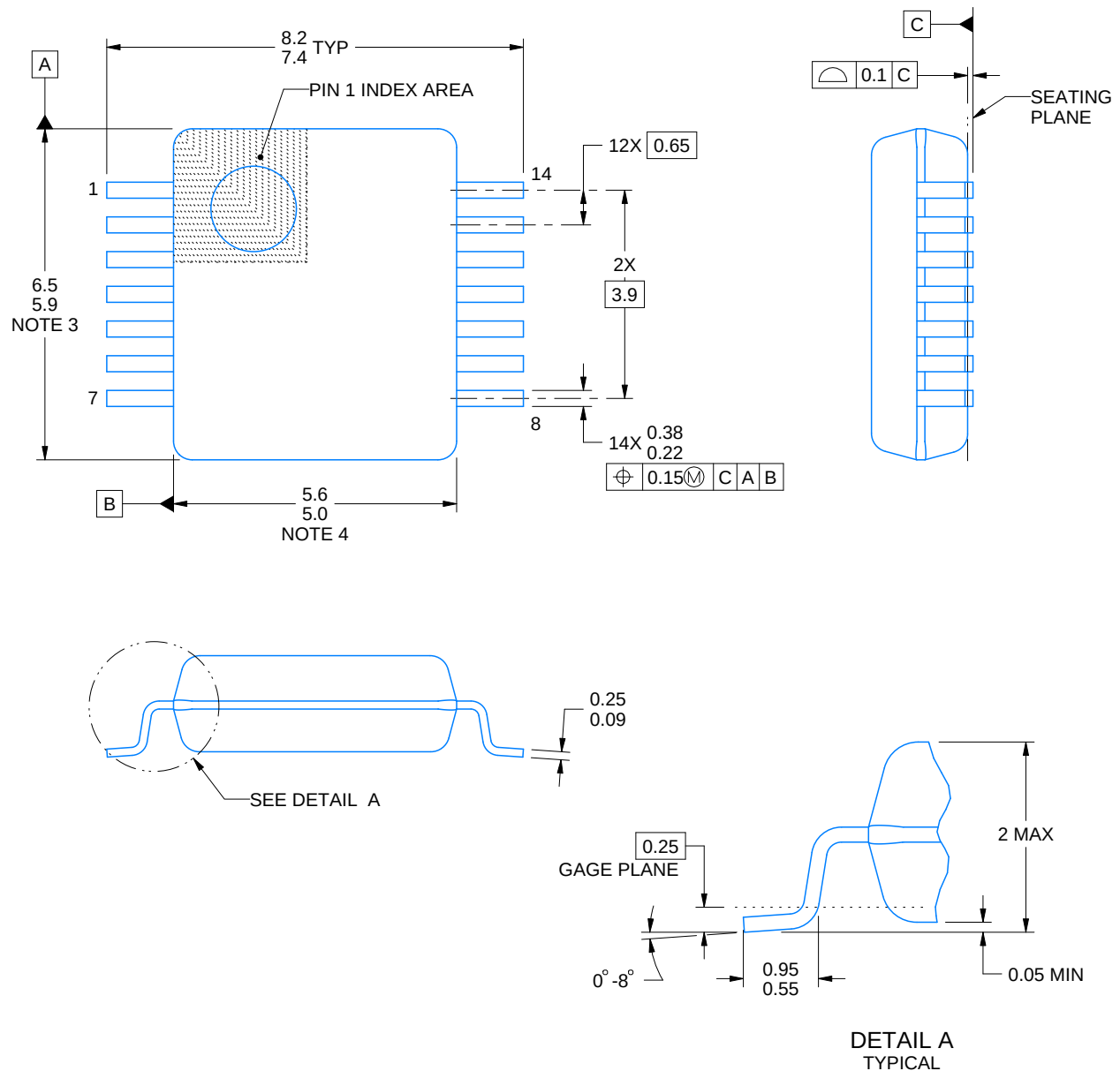
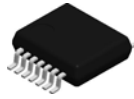
W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



4220762/A 05/2024

NOTES:

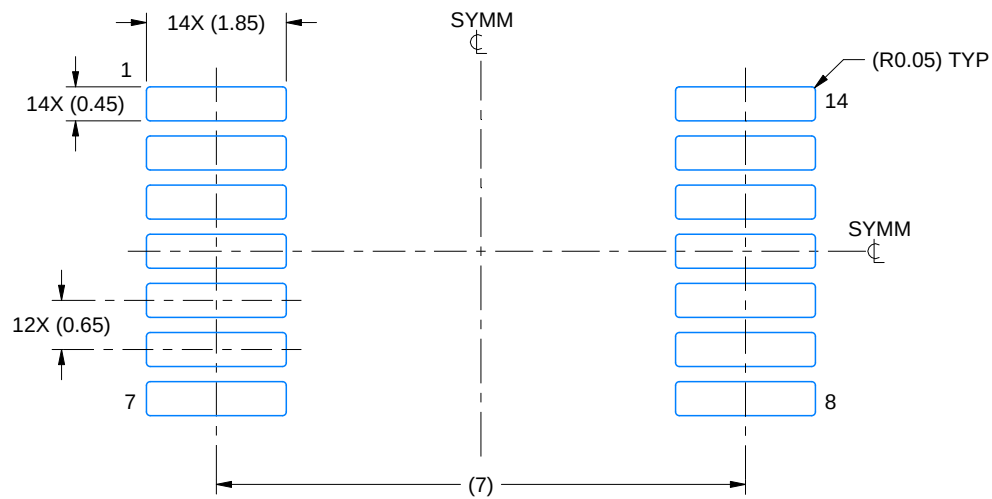
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

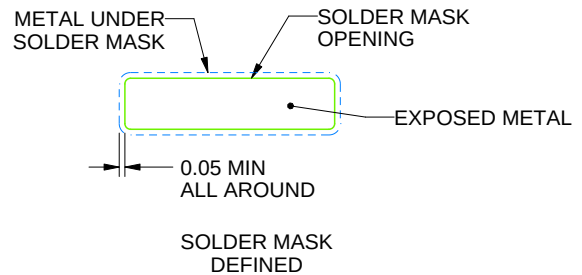
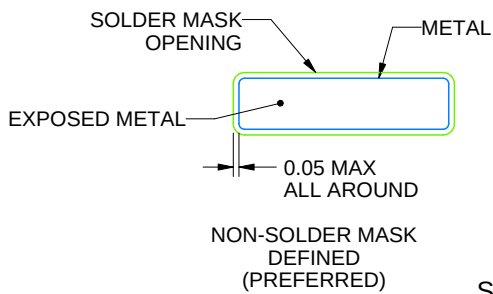
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

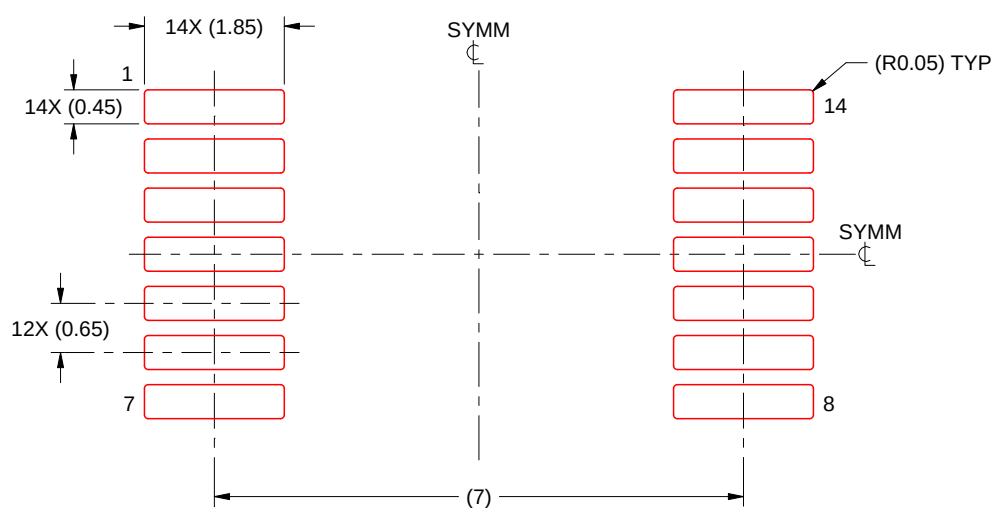
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

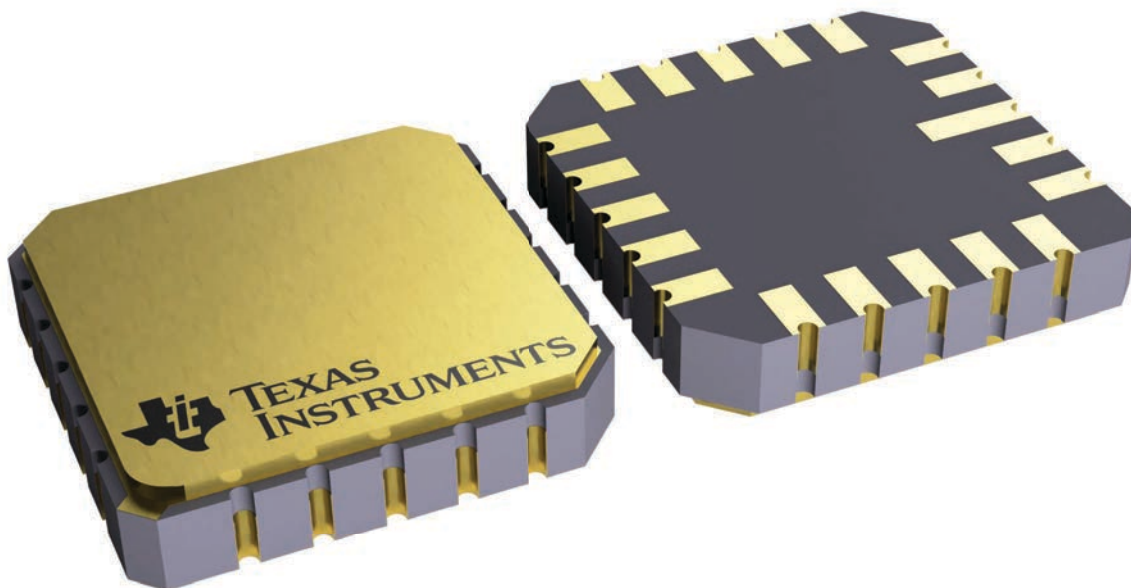
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



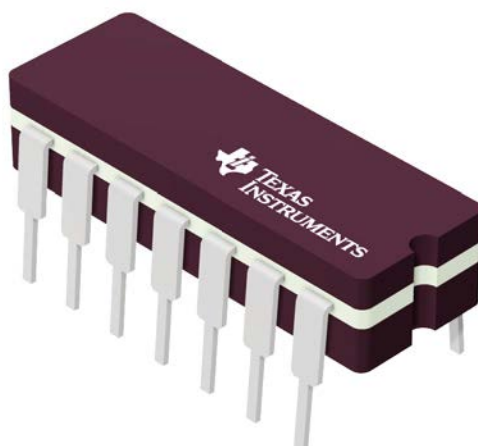
4229370VA\

J 14

GENERIC PACKAGE VIEW

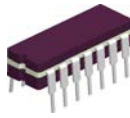
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

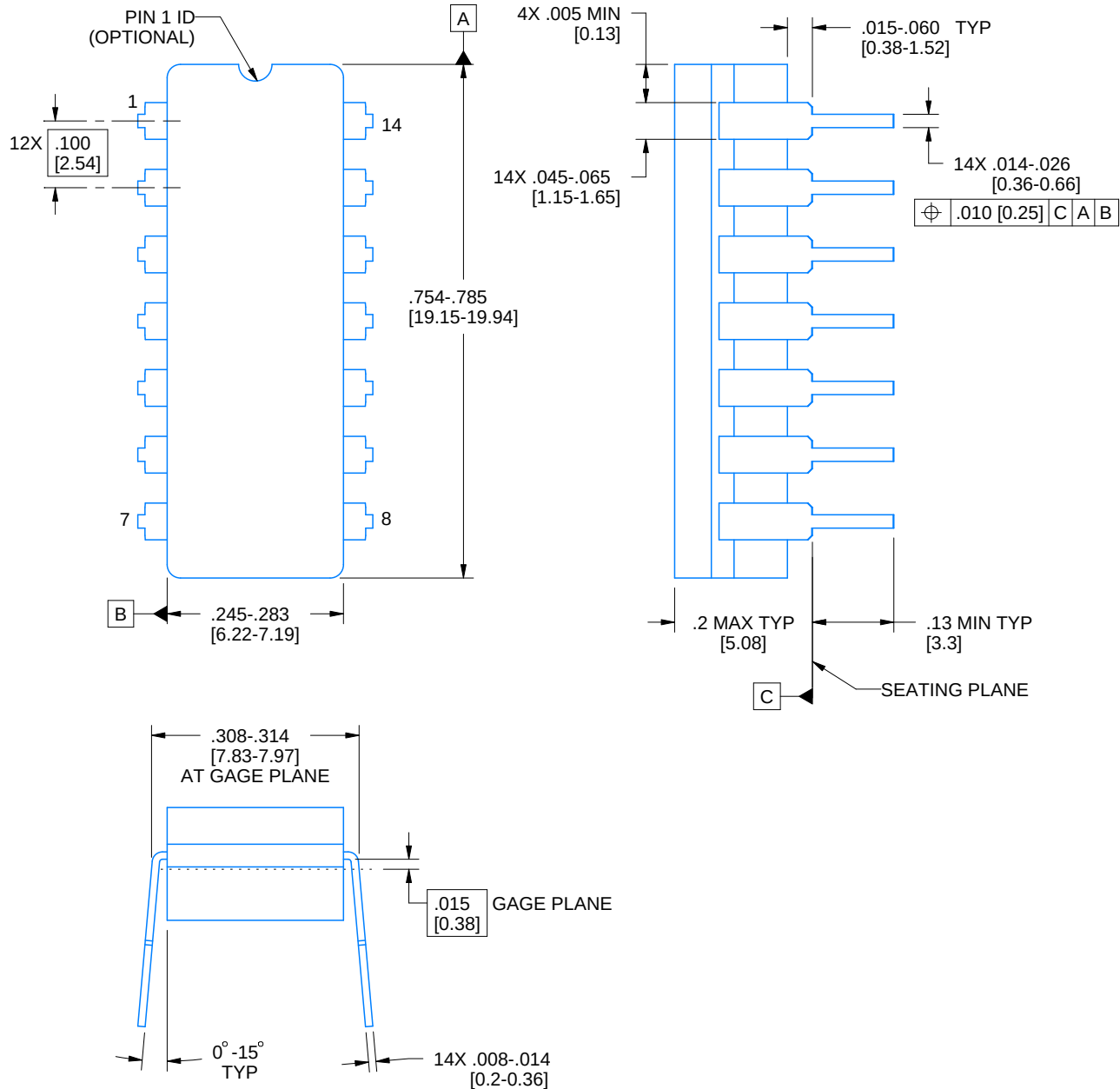


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



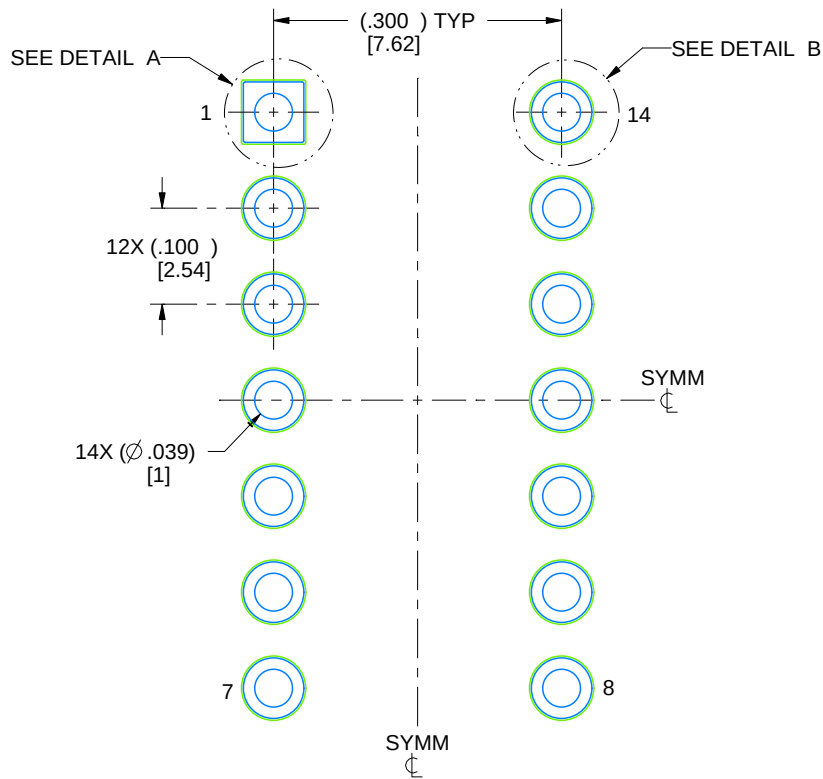
**TEXAS
INSTRUMENTS**
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EXAMPLE BOARD LAYOUT

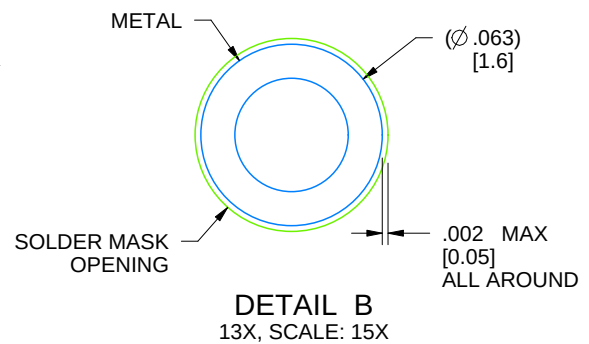
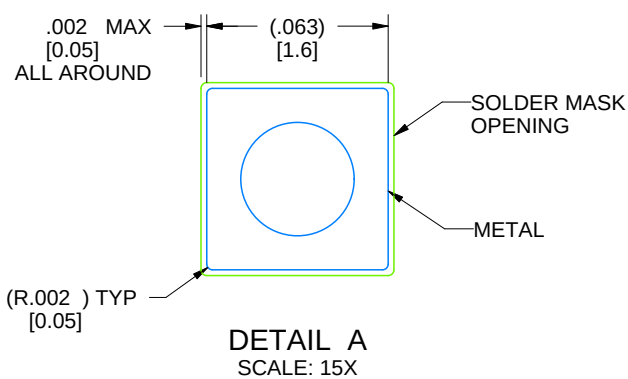
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

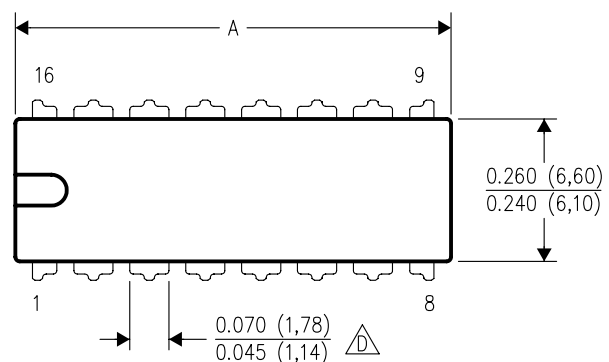


4214771/A 05/2017

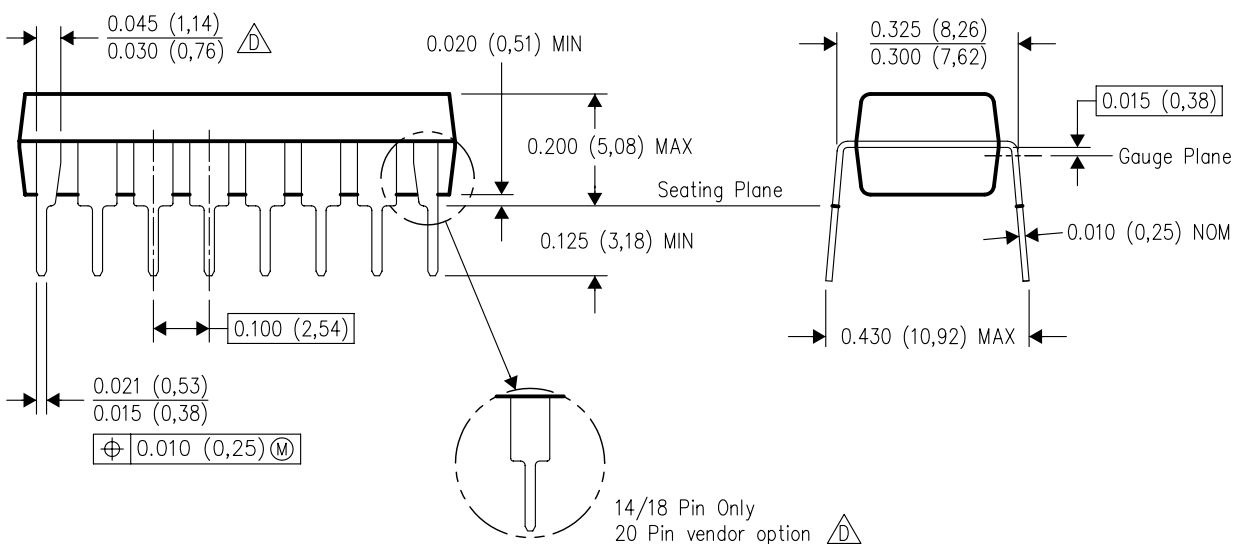
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

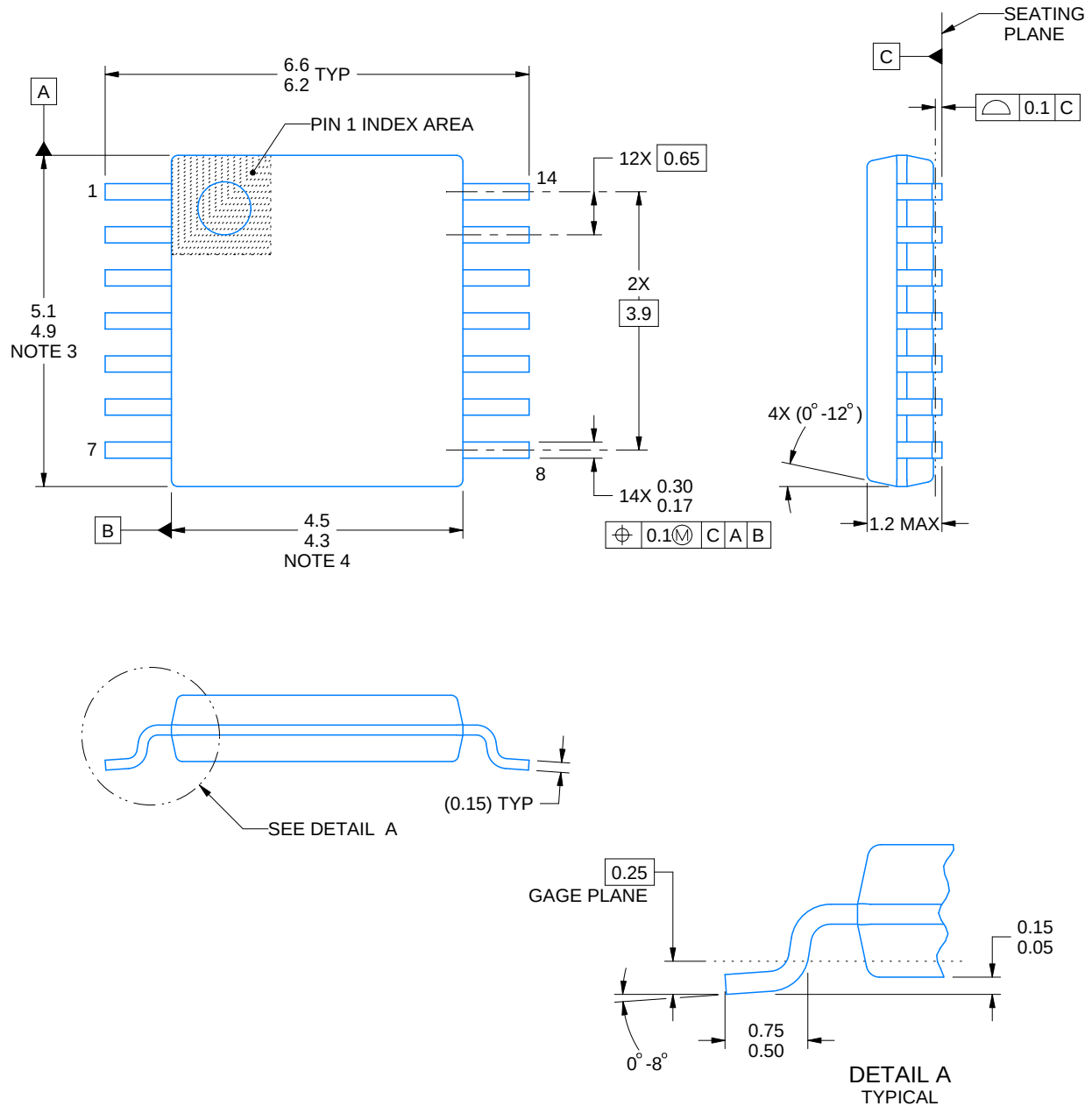
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

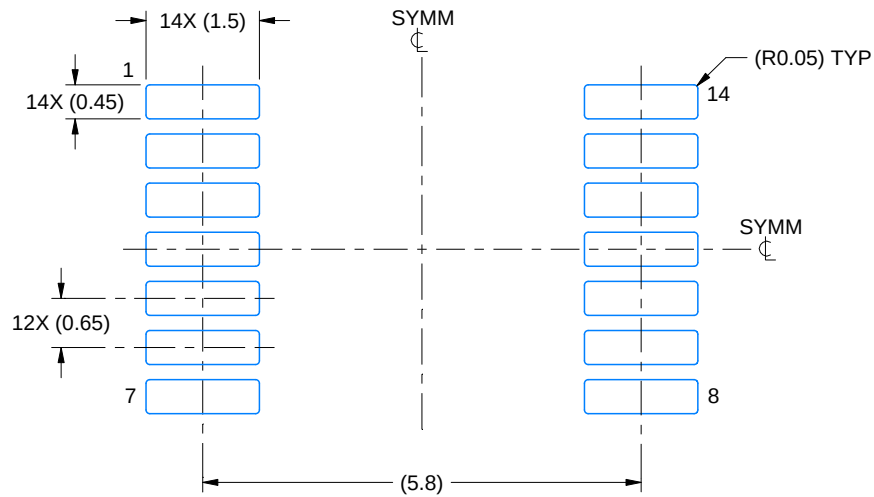
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

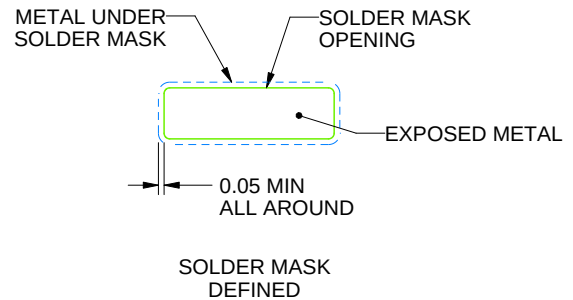
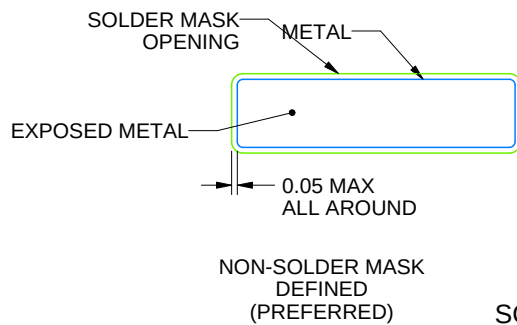
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

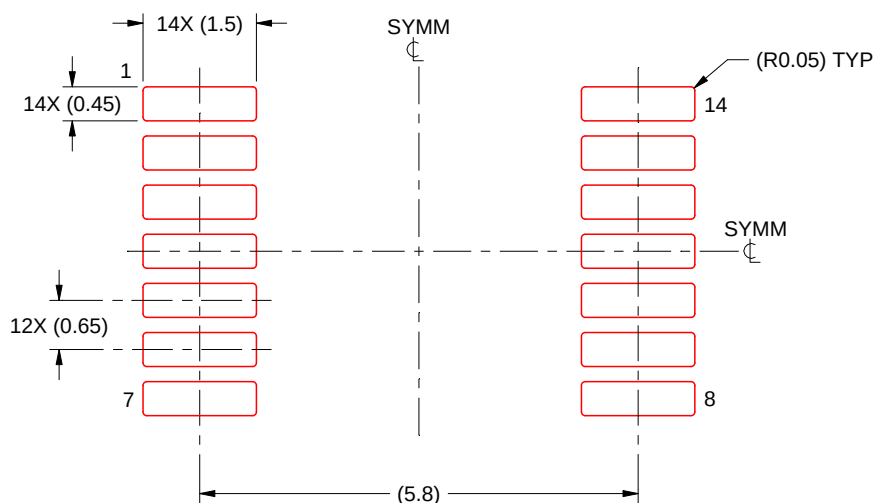
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

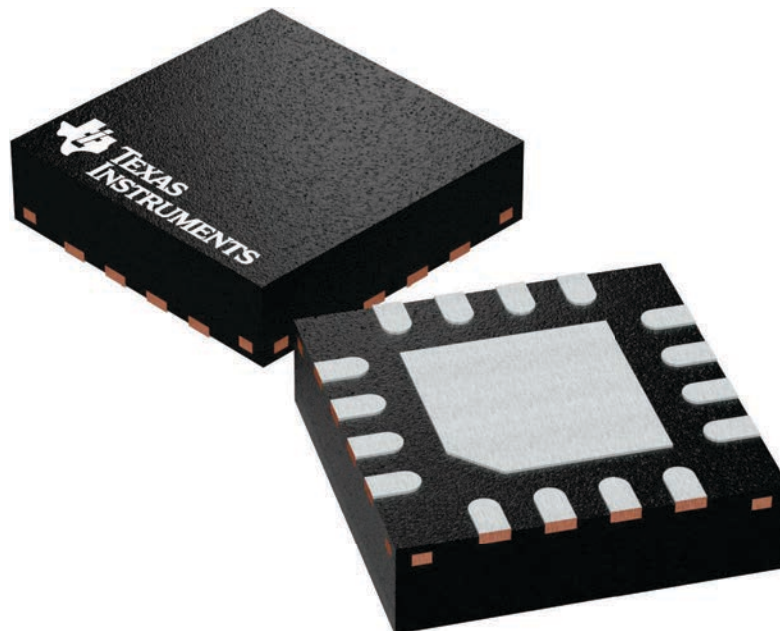
RTE 16

WQFN - 0.8 mm max height

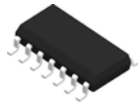
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

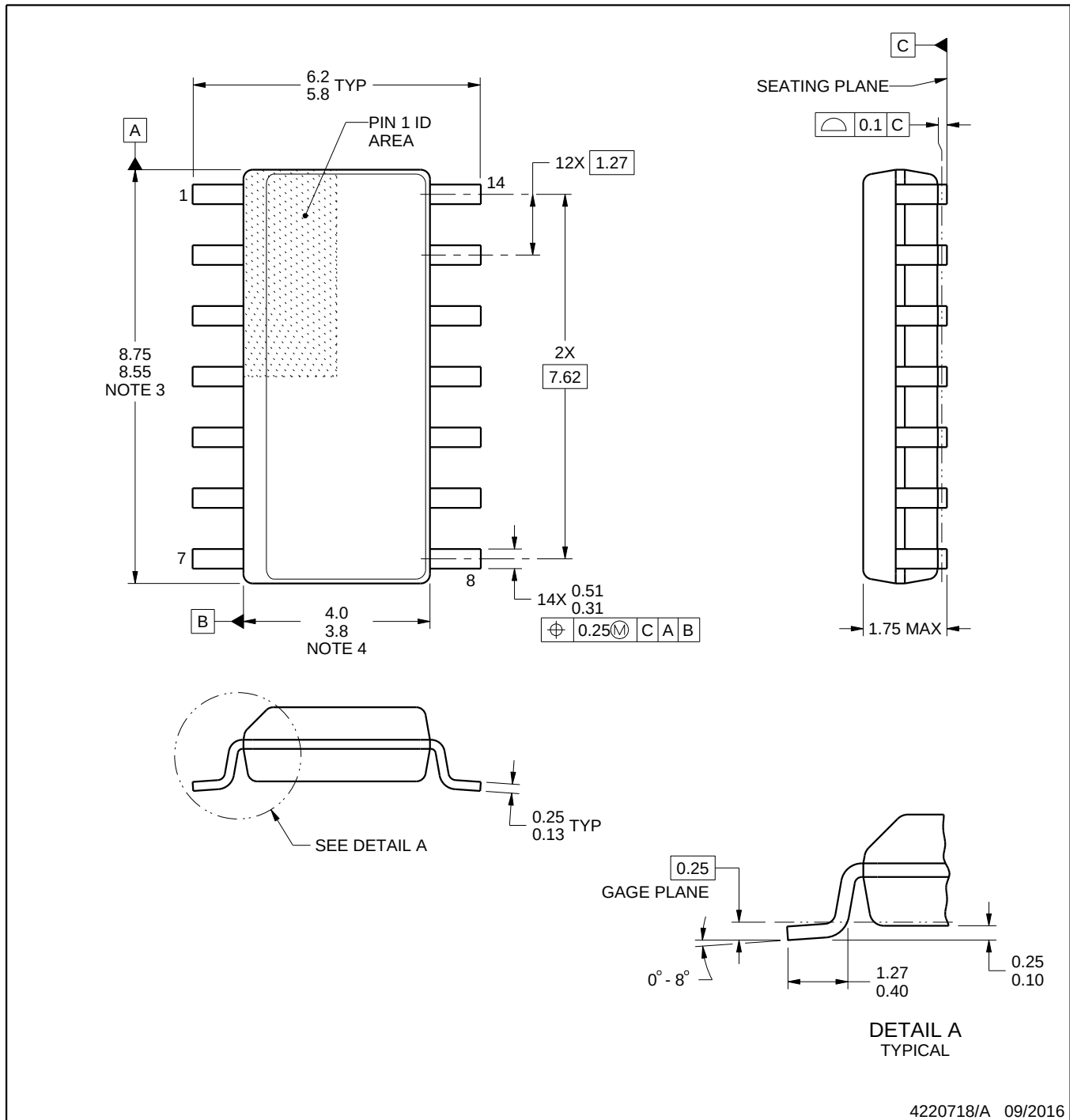
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

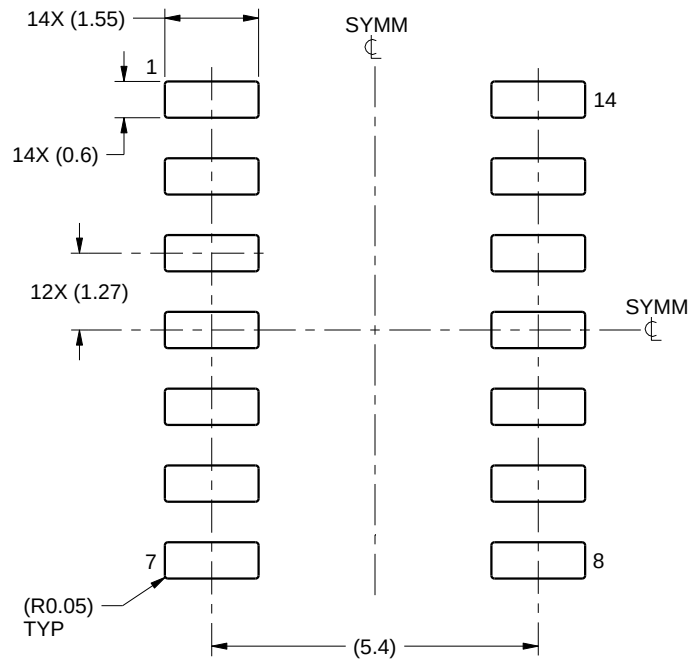
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

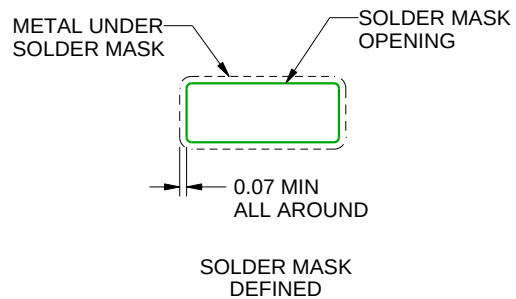
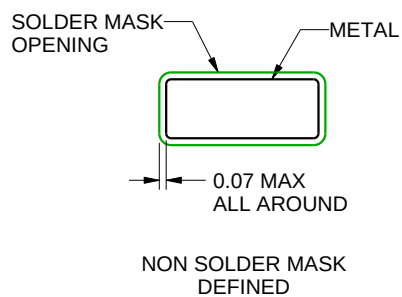
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

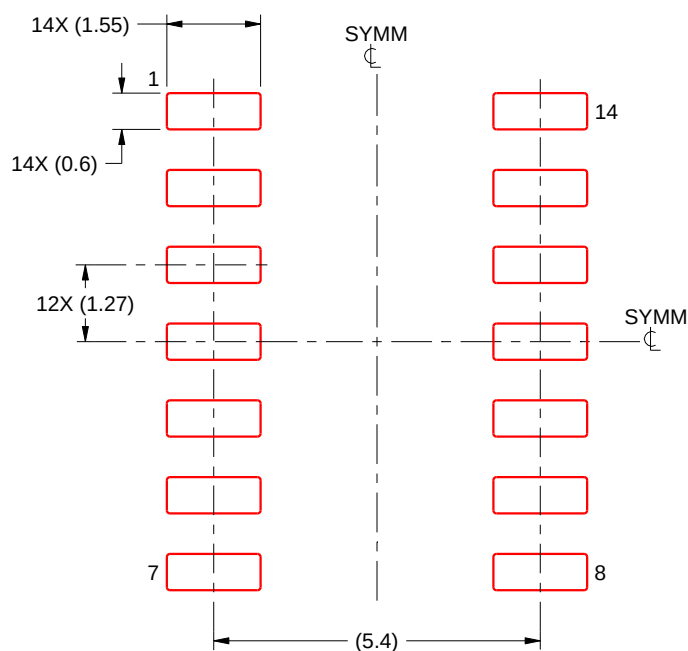
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

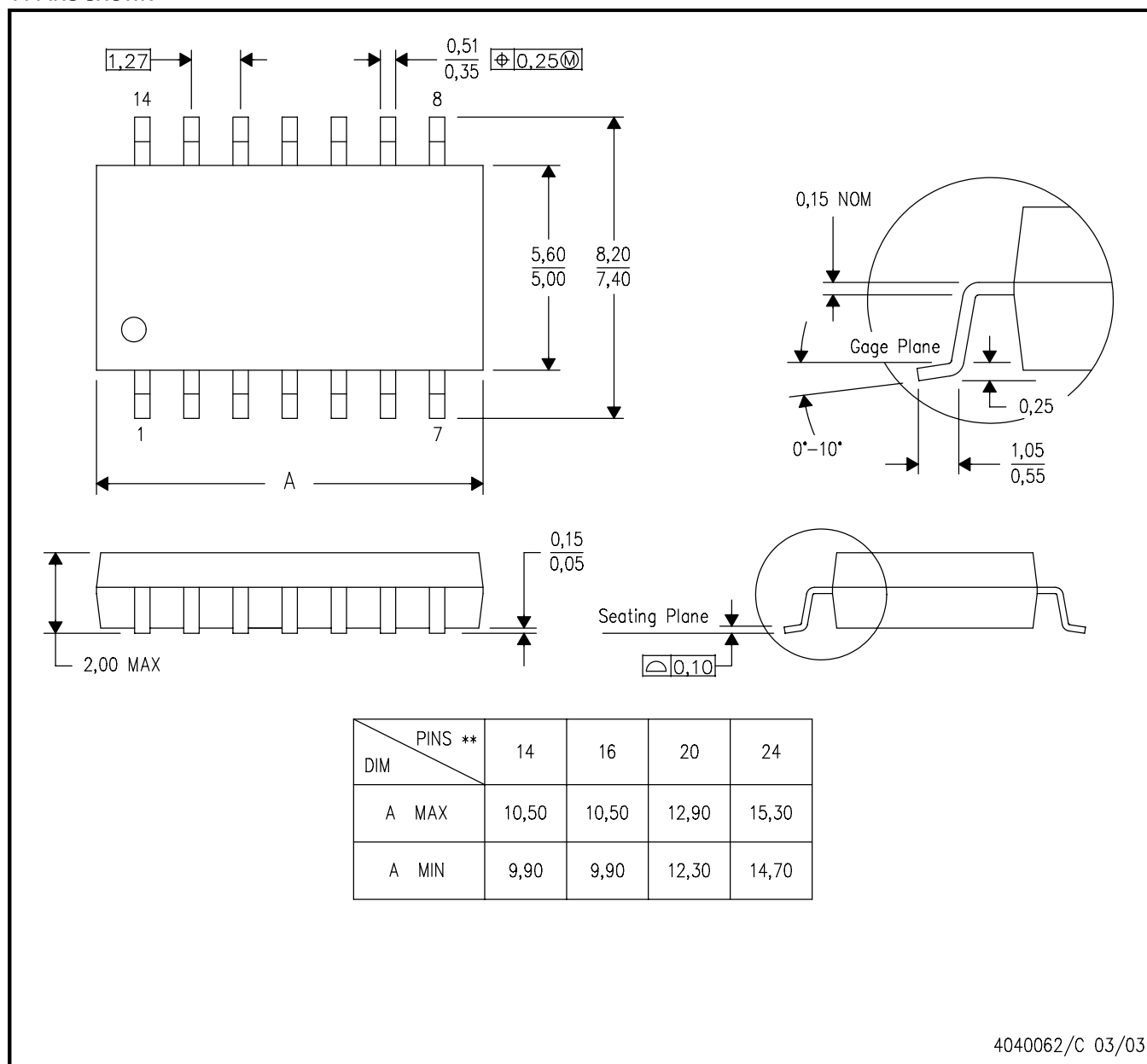
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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